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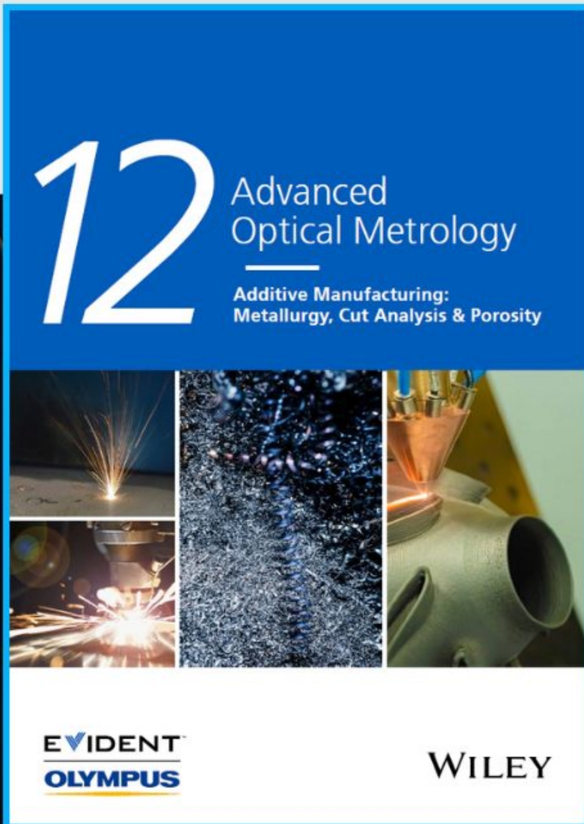

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Dual-Gated MoS_2 Memtransistor Crossbar Array

*Hong-Sub Lee, Vinod K. Sangwan, William A. Gaviria Rojas, Hadallia Bergeron, Hye Yun Jeong, Jiangtan Yuan, Katherine Su, and Mark C. Hersam**

Memristive systems offer biomimetic functions that are being actively explored for energy-efficient neuromorphic circuits. In addition to providing ultimate geometric scaling limits, 2D semiconductors enable unique gate-tunable responses including the recent realization of hybrid memristor and transistor devices known as memtransistors. In particular, monolayer MoS_2 memtransistors exhibit nonvolatile memristive switching where the resistance of each state is modulated by a gate terminal. Here, further control over the memtransistor neuromorphic response through the introduction of a second gate terminal is gained. The resulting dual-gated memtransistors allow tunability over the learning rate for non-Hebbian training where the long-term potentiation and depression synaptic behavior is dictated by gate biases during the reading and writing processes. Furthermore, the electrostatic control provided by dual gates provides a compact solution to the sneak current problem in traditional memristor crossbar arrays. In this manner, dual gating facilitates the full utilization and integration of memtransistor functionality in highly scaled crossbar circuits. Furthermore, the tunability of long-term potentiation yields improved linearity and symmetry of weight update rules that are utilized in simulated artificial neural networks to achieve a 94% recognition rate of hand-written digits.

1. Introduction

The increasing demand for digital data processing and communication is pushing conventional computer architectures to their power consumption limits, resulting in the active development of energy-efficient alternative paradigms, such as neuromorphic computing.[1] In turn, novel devices beyond complementary metal-oxide-semiconductor field-effect transistors are being pursued for hardware implementation of neuromorphic computing.[2] Among the most promising base elements of artificial neural networks (ANNs) are memristive devices and synaptic transistors.[1c,3] With large resistive switching ratios, these devices are not only useful as nonvolatile memory elements but also as neuromorphic systems that can store synaptic weights in ANNs with rapid updating (i.e., learning) and efficient classification (i.e., inference) functionality.[4] While a significant advantage of memristors is their scalability via crossbar arrays, this same architecture also imposes two major challenges.[3a,5] First, the learning rule (i.e., weight update scheme) is set in the material processing step with no further control during computation. Second, reliable access to individual nodes in a crossbar architecture requires a nonlinear (i.e., diode) or active (i.e., transistor) component at each node, limiting scaling to the same level as conventional dynamic random access memory.

To overcome these challenges, novel memristive systems are being investigated, such as complementary resistive switching and the integration of synaptic transistors with diffusive memristors.[3d,6] However, synaptic transistors do not offer control over learning rate and require an additional element at each node for individual device access in a crossbar architecture since their nonvolatile resistance states are written by a gate bias and read by a drain current.[3d,7] Thus, despite being a three-terminal device, the gate terminal in a synaptic transistor is not available for additional tunability over the current–voltage characteristics. In contrast, an emerging candidate for neuromorphic hardware is the three-terminal memtransistor, where resistance states are controlled by resistive switching near the contacts via drain voltage pulses (i.e., nonvolatile operation) while the channel conductivity can be further modulated by a gate bias during reading (i.e., volatile operation).[8] This device is enabled by the weak electrostatic screening in 2D materials and van der Waals heterojunctions, which is a property that has been recently explored for tunable and biomimetic neuromorphic responses.[8a,b,9] In particular, monolayer MoS_2 has been specifically identified as a promising semiconductor by the International Technology Roadmap for Semiconductors due to a variety of attributes including favorable device metrics, stability, and scaling potential.[10]

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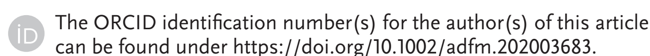
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Initial implementations of monolayer MoS_2 memtransistors showed a variety of unique functionalities including multiterminal heterosynaptic responses that are enabled by its planar architecture.[8b] However, integration of these memtransistors into scalable crossbar array architectures has not been achieved. In addition, previous implementations of memtransistors have only utilized single gate electrodes and thus have not taken full advantage of the opportunities for dual gating that have been exploited in other devices based on 2D semiconductors.[11] Furthermore, current approaches to achieve linear and symmetric weight update rules that allow higher accuracy in neural networks[12] have relied on modifications to materials composition or complex voltage pulsing schemes, both of which limit overall performance and speed.[13] Recognizing these unfulfilled opportunities, we report here the fabrication, characterization, and integration of dual-gated monolayer MoS_2 memtransistors into crossbar arrays. Dual-gated memtransistors provide facile control over a range of neuromorphic responses including multiple intermediate resistance states and gate-tunable long-term potentiation and depression synaptic behavior. This gate tunability enables improved linearity and symmetry of the synaptic response, which achieves efficient classification of hand-written digits using an ANN. In addition, dual gating allows for addressability of individual nodes in crossbar arrays without the sneak current and crosstalk issues that plague traditional memristor crossbar architectures. Since the two gate lines reside in separate processing layers, the dual-gate design possesses the same footprint and scaling limits of single-gated memtransistors. Overall, this work demonstrates that four-terminal dual-gated memtransistors enable unique neuromorphic functionality and crossbar array integration advantages compared to two-terminal memristors and three-terminal single-gated memtransistors.

2. Dual-Gated MoS_2 Memtransistor Characteristics

The two gates in dual-gated memtransistors can be conceptualized as modulatory terminals in biological neurons (**Figure 1**a,b), which provide non-Hebbian learning functionality, such as heterosynaptic plasticity and homeostatic plasticity.[14] These complex learning protocols are desired in ANNs to mitigate overshooting of individual synaptic weights and to achieve greater network stability during the training stage. Toward this end, dual-gated MoS_2 memtransistors were fabricated on polycrystalline monolayer MoS_2 grown by chemical vapor deposition (CVD). The devices use a global bottom gate and local top gate as shown in Figure 1c. Specifically, polycrystalline monolayer MoS_2 was grown by CVD on doped Si substrates coated with 300 nm thick thermal oxide serving as the bottom gate dielectric. The quality of the monolayer MoS_2 was confirmed by atomic force microscopy, Raman microscopy, photoluminescence spectroscopy, and X-ray photoelectron spectroscopy (see Figures S1 and S2, Supporting Information). Source and drain electrodes were then patterned on the continuous MoS_2 film by electron-beam lithography, followed by etching of the MoS_2 into memtransistor channels via reactive ion etching. Atomic layer deposition (ALD) of Al_2O_3 was

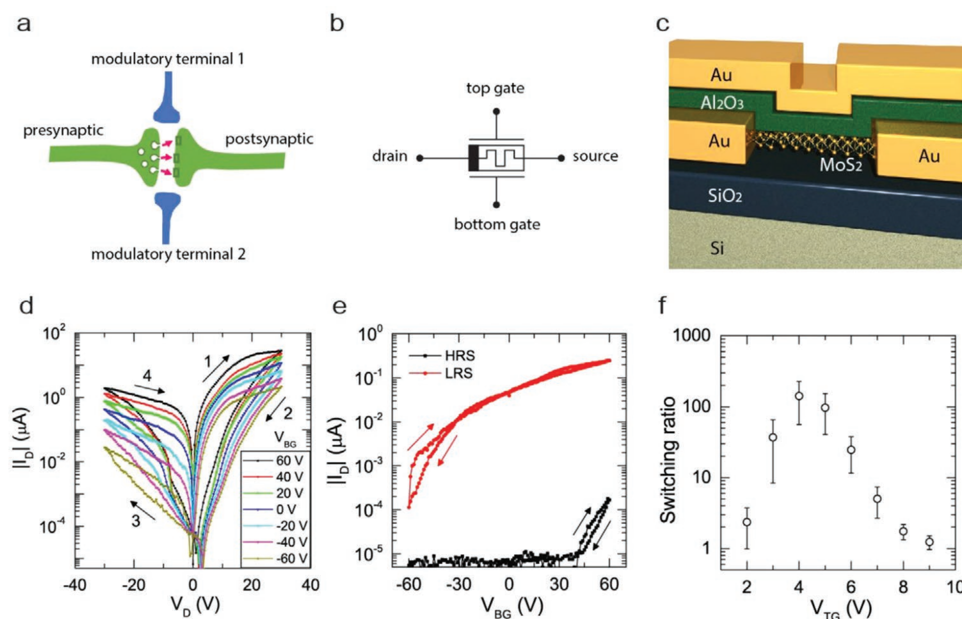

Figure 1. Architecture and characteristics of the dual-gated MoS_2 memtransistor. a) Schematic of synaptic connections between neurons with two modulatory terminals for controlled release of neurotransmitters. b) Electrical symbol of a dual-gated memtransistor where the two gates act as modulatory terminals. c) Schematic of the dual-gated MoS_2 memtransistor structure. The Si substrate acts as a global bottom gate and patterned Au acts as a local top gate. d) Gate-tunable memristive switching ($V_D = \pm 30$ V) at various bottom gate biases (V_{BG}) from −60 to 60 V with the top gate floating ($L = 0.9$ µm, $W = 0.7$ µm). The black arrow and number indicate the bias sweep sequence (clockwise switching). e) Transfer curve ($V_D = 1$ V) as a function of V_{BG} for the low resistance state (LRS) and high resistance state (HRS) of the memtransistor. The arrows indicate the gate bias sweep sequence. f) Nonmonotonic tunability of the switching ratio ($V_D = 1$ V) with respect to the top gate bias V_{TG} ($V_{BG} = -60$ V). The error bars represent the standard deviation of 20 memtransistor devices.

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used to deposit a top gate dielectric of 30 nm in thickness, followed by patterning of local top gate contacts (see Figure S3, Supporting Information).

Figure 1d shows the bipolar resistive switching characteristics of the dual-gated MoS_2 memtransistor at different bottom gate biases (V_{BG}) with a floating top gate. The device channel dimensions of all individual and crossbar devices are identical (channel length, $L = 0.9$ µm; channel width, $W = 0.7$ µm). The device is initially in a low resistance state (LRS) and switches to a high resistance state (HRS) at forward bias (drain voltage $V_D > 0$). This RESET process (i.e., switching from LRS to HRS) occurs during both sweeps 1 and 2 in Figure 1d. In contrast, the device undergoes a SET process (i.e., switching from HRS to LRS) at reverse bias ($V_D < 0$). It should be noted that SET and RESET do not require an electroforming process. As a result, dual-gated memtransistors show a pinched hysteresis loop in the clockwise direction at forward bias, in contrast to the counter-clockwise loops for single-gated MoS_2 memtransistors (bottom gate or top gate).[8b,9c] It should be noted that the large memristive loop (Figure 1d) with minimal bottom gate bias hysteresis (Figure 1e; and Figure S4, Supporting Information) also distinguishes a memtransistor from a synaptic transistor.[7c,9g] Both the direction of switching and the rectification polarity suggest that the dominant resistive switching is occurring at the forward-biased Schottky diode (for $V_D > 0$ V) near the drain contact as opposed to the reverse-biased Schottky diode near the source contact that was observed in single-gated memtransistors.[8b] The opposite switching direction between single-gated and dual-gated memtransistors likely originates from resistive switching occurring at opposite electrodes (source vs drain) as will be discussed in more detail below.

The low-bias transconductance and threshold voltage (V_{TH}) undergo substantial changes between HRS and LRS. In LRS, the dual-gated memtransistor does not turn off even at $V_{BG} = -60$ V, while no measurable current was observed in HRS up to $V_{BG} = 40$ V. The RESET and SET operations were also achieved with lower operating voltages ($V_D = \pm 30$ V) than previously reported single-gated memtransistors ($V_D = \pm 50$ V),[8b] as would be expected for the smaller L (<1 µm) and thinner top gate dielectrics compared to previous single-gated memtransistors (L = 5–15 µm).[8b] The top gate voltage (V_{TG}) further controls the resistive switching ratio in a nonmonotonic fashion (Figure 1f). On the other hand, the resistive switching ratio increases with V_{BG}, which is the opposite of the gate-tunability observed in single-gated memtransistors (Figure S5, Supporting Information).[8b] This opposite behavior is explained by a different switching mechanism as discussed below. The hysteresis is maximum at $V_{TG} = 4$ V and decreases for $V_{TG} < 4$ V due to the overall smaller drain current in the subthreshold regime. The hysteresis decreases for $V_{TG} > 4$ V because an overall decreased Schottky barrier height in the accumulation regime also results in a smaller modulation of the barrier height during memristive switching.

Scaling to smaller L (and lower V_D) in these memtransistors is enabled by the smaller average grain size (≈1 µm) in this case (see the Supporting Information). However, the operating voltage is not expected to scale linearly with L due to the dominance of thermionic emission and space-charge effects near the Schottky contacts. Further scaling could be achieved by growing even smaller grains or patterning postgrowth lattice defects as has been shown with focused ion-beam irradiation for MoS_2 memtransistors on single-crystal flakes.[15] Point defects are also known to play a critical role in vertical memristors based on monolayer, bilayer, and few-layer MoS_2.[16] The detailed role of lattice point defects in the memristive I–V characteristics of MoS_2 devices can likely be revealed by atomically resolved in situ scanning tunneling microscopy[17] or scanning transmission electron microscopy.[8a,18]

The dual-gated MoS_2 memtransistors show excellent cycle-to-cycle endurance, as shown by the tight distribution of switching characteristics for 250 bias sweeps (**Figure 2**a) and stable resistance values in HRS and LRS (Figure 2b). The I–V characteristics do not pass through $V_D = I_D = 0$ in Figures 1d and 2a, which is a result of a mem-capacitive effect that is known to induce a pinched hysteresis loop in the charge–voltage plot as opposed to the current–voltage plot.[19] This mem-capacitive effect is expected near the metal contacts as has been previously observed in MoS_2 memristors[20] and single-gated MoS_2 memtransistors.[8b] Figure S6 (Supporting Information) shows the endurance of a dual-gated MoS_2 memtransistor through its final breakdown event. In this case, the endurance is limited by the large applied biases (±30 V) chosen to maximize the switching ratio but also approach the breakdown voltage of the top-gate. In practice, the bias range would be limited to improve endurance while still maintaining a switching ratio within an acceptable range for neuromorphic applications. Characterization of 54 memtransistors showed qualitatively similar behavior with low variability in switching ratio among the tested devices (discussed in Figure 5). The endurance of the same memtransistor at different V_{BG} values ranging from 60 to −60 V further shows minimal deviation for the intermediate resistance states that are accessible through bottom gate bias modulation (Figure S7, Supporting Information). Both the HRS and LRS states show long retention with extrapolated switching ratios over 10^2 on the timescale of years (Figure 2c; and Figure S8, Supporting Information). Intermediate resistance states between HRS and LRS can also be achieved through voltage pulsing with similarly stable retention behavior (Figure 2d). Further estimates of the intrinsic timescale of memory states can be made by long-term temperature-dependent retention measurements, as has been done for metal-oxide memristors.[21] It should be noted that the utility of intermediate states in networks of memtransistors also relies on low device-to-device variability.[3d] However, dual-gated MoS_2 memtransistors have the advantage of fine-tuning the resistance states via gate bias pulses to offset variability in the long-term memory.

Next, we discuss the potential switching mechanisms. As previously mentioned, the clockwise switching direction and its inverted rectification polarity are consistent with dominant resistive switching at the drain electrode. Since the devices do not show gate leakage current (<0.2 nA) for HRS or LRS while sweeping either V_{BG} or V_{TG} after high-bias memtransistor measurements (Figure S9, Supporting Information), dielectric breakdown and direct tunneling between the channel and gate electrodes can be ruled out during switching. However, a drain bias of 30 V could potentially produce a sufficiently high electric field to inject electrons into the mid-gap states of the Al_2O_3 top dielectric that are just above the MoS_2 conduction band edge.[22] To further elucidate the switching mechanism, we note that

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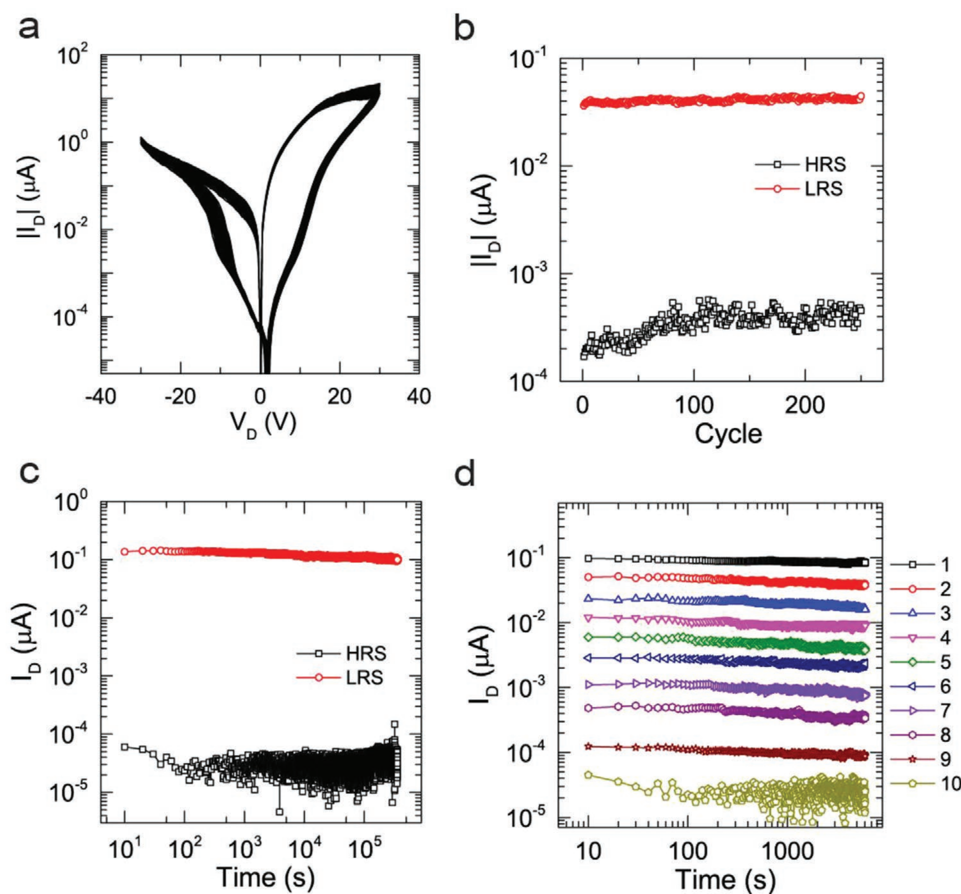

Figure 2. Endurance and retention characteristics of dual-gated MoS_2 memtransistors. a) A plot of 250 full switching cycles at $V_{BG} = 0$ V and $V_{TG} = 0$ V. b) Corresponding LRS and HRS values for the 250 full switching cycles of part a). I_D values were extracted at $V_D = -2$ V to avoid the nonzero crossing at $V_D = 2$ V that resulted in negative I_D. c) Retention behavior of the LRS and HRS states for 24 h where the device was measured at $V_D = 2$ V every 10 s (see Figure S8 for retention time extrapolation, Supporting Information). d) Retention behavior of ten distinct resistance states during the long-term depression (LTD) of a dual-gated memtransistor. The data labeled as "1" and "10" in the legend are the LRS and HRS states, respectively. The current, I_D, was measured at $V_D = 2$ V. All subsequent current levels (2–10) were measured at the same V_D bias after writing with 1 ms wide pulses of $V_D = 20$ V. $V_{TG} = V_{BG} = 0$ V during reading and writing operations.

the dual-gated devices show distinct charge transport regimes (**Figure 3**) in contrast to the gradual changes in I_D observed during switching of single-gated MoS_2 memtransistors.[8b] The distinct segments of the *I*–*V* curves exhibit well-defined power-law behavior (i.e., $I \propto V^m$) with clear transition points (i.e., kinks) reminiscent of complex oxide memristors.[23] Here, the absence of low-bias ohmic behavior (where $m \approx 1$) is explained by the nonzero-crossing behavior resulting from mem-capacitive effects near the contacts. An exponent $m = 2$ can be explained by both space-charge-limited current (SCLC) without any traps or with a single shallow trap state, whereas an exponent $m > 2$ corresponds to an exponential density of trap states as observed in MoS_2 transistors.[24] Thus, the $I \propto V^2$ behavior transitions to a trap-filled limit (TFL) of $I \propto V^{12.5}$ at a high bias ($V_D \approx 10$ V at HRS during both SET and RESET processes), where the field is large enough to access deeper traps within MoS_2 or Al_2O_3 (Figure 3).[23a] Once most of the traps are filled, the transport resembles the trap-free case of Child's law such that the *I*–*V* characteristic reverts to a smaller value of $m = 4$–6 at higher biases ($V_D > 15$ V). This high bias asymmetry ($I \propto V^4$ in forward vs $I \propto V^6$ in reverse bias) suggests different kinetics of trap filling and emptying that is ultimately responsible for the memristive loop.[23a]

Clockwise switching results from resistive switching occurring at forward-biased Schottky contacts in the dual-gated memtransistor. Growth of high-κ metal-oxide dielectrics is known to increase electron doping of MoS_2 (and other transition metal dichalcogenides)[22,25] resulting in doping-induced lowering of the Schottky barrier height.[26] Thus, devices start in LRS and gradually switch to HRS through reversible changes near the drain contact for $V_D > 0$ V and source contact for $V_D < 0$ V. Indeed, SCLC and TFL currents during resistive switching in symmetric $Pt/TiO_2/Pt$ memristors are correlated with filamentary switching near the anode electrode (i.e., the drain electrode in memtransistor).[23b] The polarity of rectification (overall higher currents for $V_D > 0$ V compared to $V_D < 0$ V) contrasts that of a conventional Schottky transistor and single-gated memtransistor, suggesting current bottlenecks occurring at the forward-biased contacts.[8b] Two additional pieces of evidence corroborate this mechanism: 1) nonzero-crossing in I_D–V_D characteristics occurs at $V_D > 0$ V in dual-gated memtransistors as opposed to $V_D < 0$ V in single-gated

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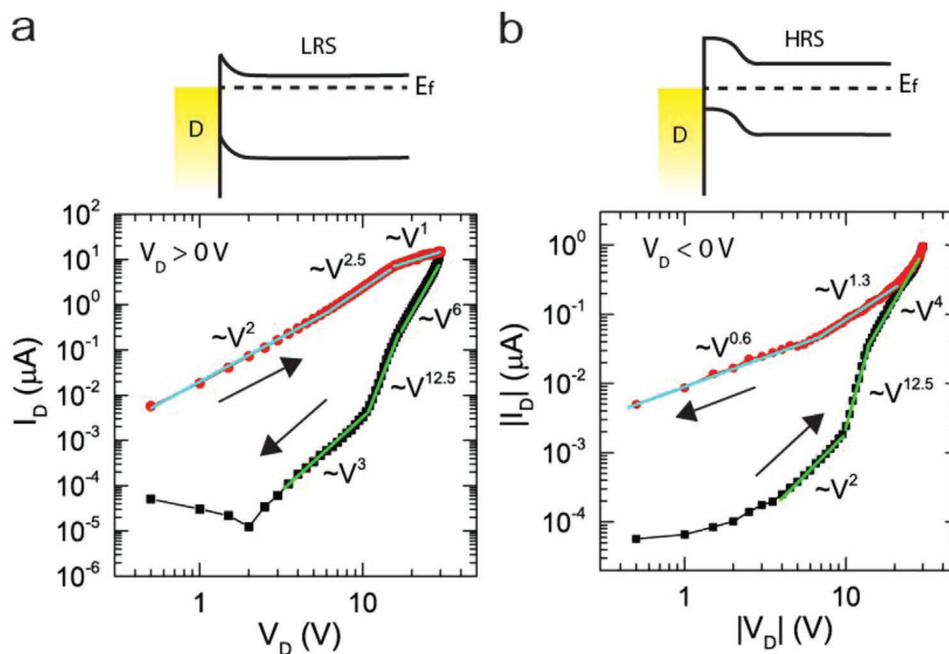

Figure 3. a) Top: Schematic diagram showing a Schottky contact and MoS_2 band-bending near the drain electrode in LRS. E_f is the Fermi energy level. Bottom: Log–log plot of I_D–V_D characteristics of a dual-gated MoS_2 memtransistor in forward bias ($V_D > 0$) showing different transport regimes during resistive switching between LRS and HRS (V_{BG} = 0 V and V_{TG} = 0 V). The power-law behavior (I–V^m) is shown at different segments of the curves. b) Top: Schematic diagram showing the increased space-charge region near the drain electrode in HRS. Bottom: Log–log plot of absolute values of I_D and V_D of the same device in reverse bias ($V_D < 0$) showing different transport regimes during resistive switching between HRS and LRS.

memtransistors (Figures 1d and 2a);[8b] 2) memristive switching ratio increases (decreases) with V_{BG} in dual-gated (single-gated) memtransistors (Figure S5, Supporting Information).

Physically, the reversible changes near the drain contact could include defect migration within MoS_2 or charge trapping in MoS_2 or Al_2O_3 as they all could contribute to the TFL transport regimes. Indeed, ALD-grown amorphous Al_xO_y has been shown to have mid-gap states slightly above the MoS_2 conduction band and is accessible for trapping at relatively low biases.[22] Thermally assisted charge trapping in the oxide has also been shown to induce nonvolatile memory effects.[27] On the other hand, recent computational work on MoS_2 memtransistors also predicts that the diffusion barrier of sulfur vacancies in MoS_2 can be as low as 0.68 eV, resulting in a significant hopping rate (>10^2 s^{-1}) that increases rapidly with increasing temperature.[9c] Similarly, local Auger electron spectroscopy of MoS_2 memristors demonstrated decreased sulfur content near contacts during switching.[9d] The net outcome is a significant space-charge region near the drain contact that induces band-bending in MoS_2 at zero drain bias, ultimately resulting in nonvolatile memristive switching (Figure 3).

3. Gate-Tunable Plasticity

In biological systems, the synaptic connections between neurons are strengthened through repeated firing, and similar concepts are used to train spiking neural networks. However, it is also understood that modulatory terminals in biological systems further control the synaptic connections.[14a,b,28] Similarly, the two gate terminals in dual-gated memtransistors provide electrostatic control over synaptic learning behavior. As shown in **Figure 4**, tunable learning is achieved in long-term potentiation (LTP) and long-term depression (LTD) for dual-gated memtransistors, where V_D pulses of 1 ms period are applied and the postsynaptic current (I_{PSC} = I_D) is measured between pulses. For simplicity, the top gate is grounded in all measurements, while the bottom gate voltage is controlled during the reading and writing operations (in principle, these roles of the bottom and top gates can be reversed). As expected from the direction of switching (Figure 1d), positive V_D pulses induce LTD and negative V_D pulses induce LTP. For LTD, the memtransistor is subjected to V_D pulses (20 V) at different V_{BG} writing voltages $V^W{}_{BG}$, and the changed resistance states are probed at a low bias (V_D = 1 V) at different V_{BG} reading voltages $V^R{}_{BG}$ (Figure 4a). Figure 4b,c shows two writing operations at $V^W{}_{BG}$ = 60 and –60 V, respectively, where each state was further read at a different $V^R{}_{BG}$ ranging from 60 to 0 V. For $V^W{}_{BG}$ = $V^R{}_{BG}$ = 60 V, I_{PSC} is reduced by 100-fold in just 10 pulses (Figure 4b). In contrast, for $V^W{}_{BG}$ = –60 V and $V^R{}_{BG}$ = 60 V, I_{PSC} decreases only by a factor of two for the same number of pulses (Figure 4c). It should be noted that a slower learning rate for negative $V^W{}_{BG}$ in Figure 4c is opposite to what would be expected from previous single-gated memtransistors that show a larger switching ratio at negative V_{BG} values.[8b] In particular, dual-gated memtransistors show the opposite trend with a smaller switching ratio at negative V_{BG} values (Figure 1d; and Figure S5, Supporting Information), and overall ON and OFF currents that are lower for negative V_{BG} values. A smaller current and limited resistive switching during negative $V^W{}_{BG}$ pulses are expected to induce a

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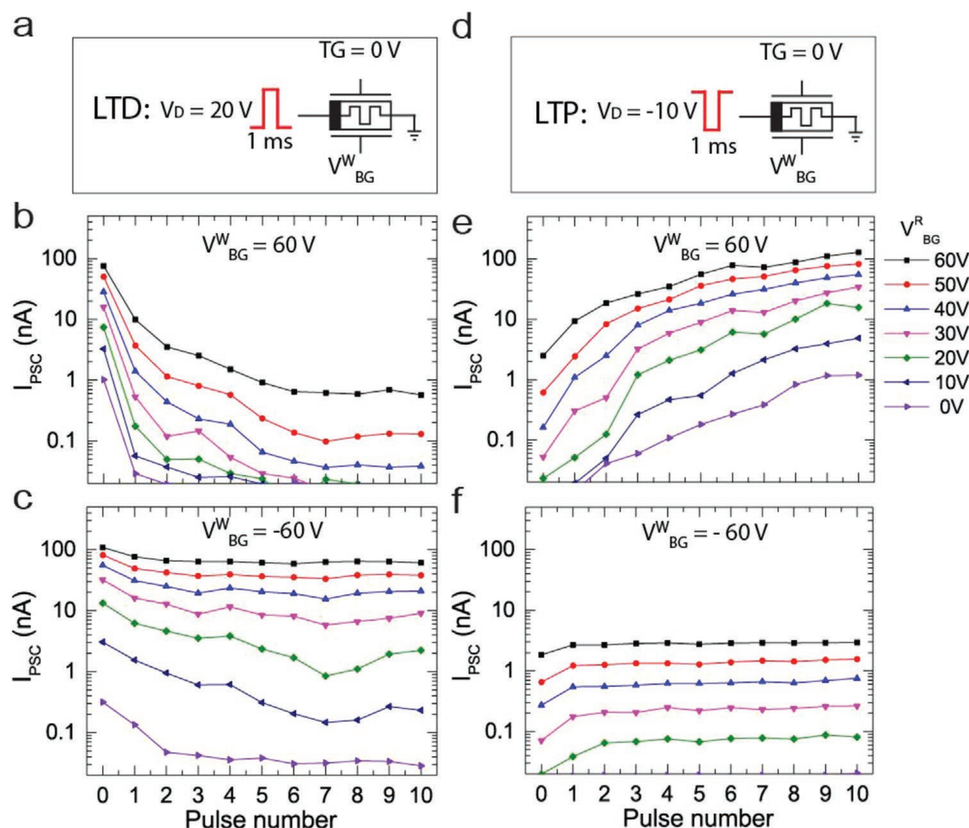

Figure 4. Tunable long-term potentiation and depression of MoS_2 dual-gated memtransistors. a) Pulsing scheme for long-term depression (LTD) at various V_{BG} values during the writing operation ($V^W{}_{BG}$). The device was read at $V_D = 1$ V and various V_{BG} values during the reading operation ($V^R{}_{BG}$). b,c) $V^R{}_{BG}$-dependent LTD behavior at $V^W{}_{BG} = 60$ and –60 V, respectively. d) Pulsing scheme for long-term potentiation (LTP) at $V^W{}_{BG}$ during the writing operation. e,f) $V^R{}_{BG}$-dependent LTP behavior at $V^W{}_{BG} = 60$ and –60 V, respectively. The legend to the right of (e) corresponds to all plots in this figure. V_{TG} was grounded throughout the LTD and LTP measurements. Exponential fits to the LTD and LTP curves in (b) and (e) are provided in Figure S10 (Supporting Information).

smaller degree of defect rearrangement near the drain contact, resulting in a slower learning behavior. Thus, the initial current values are comparable in Figure 4b,c due to the same $V^R{}_{BG}$ values, but they evolve differently with pulsing due to different $V^W{}_{BG}$ values.

Similar tunable learning is achieved in LTP using 10 pulses of $V_D = -10$ V (Figure 4d). The devices show a ≈100-fold increase in I_{PSC} for $V^W{}_{BG} = V^R{}_{BG} = 60$ V, and only a twofold increase for $V^W{}_{BG} = -60$ V and $V^R{}_{BG} = 60$ V. Thus, LTP effectively regains the original synaptic strength before LTD operation for a comparable number of pulses. The learning rate changes monotonically with decreasing $V^W{}_{BG}$ as shown by the intermediate cases with $V^W{}_{BG} = 0$ V (Figure S10a,b, Supporting Information). Reading at different $V^R{}_{BG}$ changes the absolute I_{PSC} values, but the overall learning rates are not affected significantly as shown by the exponential fits in Figure S10c,d (Supporting Information), where the characteristic decay and growth rates remain approximately constant. A smaller magnitude V_D pulse is needed for writing in LTP (–10 V) than LTD (20 V) due to the asymmetric I_D–V_D characteristics of memtransistors (Figure 1d).

We emphasize that reading the resistance state at different $V^R{}_{BG}$ values does not change the intrinsic nonvolatile resistance of the device, as expected from the lack of hysteresis in the I_D–V_{BG} characteristics (Figure 1e). This decoupling of reading and writing operations is one of the key advantages of dual-gated memtransistors since the nonvolatile memristive states remain unperturbed by $V^R{}_{BG}$ during the reading operations. However, the total device current can still be modulated by the gate biases during reading by modulating the resistance of the transistor response of the memtransistor. The energy consumption for learning steps in Figure 4 is in the range of 2 pJ to 2 nJ per operation for $V^W{}_{BG}$ from –60 to 60 V. In conventional crossbar arrays, the energy consumption scales with crossbar array size due to sneak current issues. In contrast, dual-gated memtransistor crossbar arrays are expected to minimize this excess energy consumption by minimizing sneak currents, providing another key advantage over conventional architectures. A multilevel memory effect is also demonstrated by the retention behavior of 10 distinct intermediate resistance states during an LTD operation (Figure 2d), which show qualitatively similar retention behavior as the LRS and HRS states in Figure 2c. All learning demonstrations were performed with 1 ms pulses since the speed of the memtransistors is expected to be limited by the parasitic capacitance from the global bottom gate and large metal pads used for probing (RC time constant > 10 µs). Here, global bottom gates are readily obtained from direct growth of MoS_2 on oxidized Si wafers, but the bottom gates

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could also be prepatterned by exploiting transfer methods for MoS_2, thus providing a pathway to higher operating speeds.

4. Minimizing Sneak Currents

Compared to the lateral geometry of memtransistors, an apparent advantage of conventional vertical memristors is their small footprint in crossbar arrays.[5] However, accessing individual nodes in memristor-based crossbars is a challenging task due to sneak currents, and thus the small footprint is typically compromised by at least one additional circuit element at each node.[3a] The integration of a Schottky diode or a threshold switch directly with a memristor (i.e., the one-selector-one-memristor 1S1M approach) can achieve sufficiently high nonlinearity at low biases for effective addressing in small crossbar arrays through customized reduced-voltage pulsing schemes (e.g., V/2 or V/3 schemes).[29] However, regardless of nonlinearity quality, the sneak current through neighboring nodes increases with increasing crossbar size for the 1S1M approach, compromising the energy efficiency and access time.[30] Consequently, one-transistor-one-memristor (1T1M) structures are preferred since the sneak current is much lower and does not scale with crossbar size.[12c,30c,31] Nevertheless, since memristive components in 1T1M are still limited to two terminals, tunable learning response has not yet been achieved,[32] thus motivating efforts to integrate dual-gated memtransistors into crossbar arrays.

For dual-gated memtransistor crossbar fabrication, drain bit and source lines (electrode width ≈3 µm, interline gap ≈0.9 µm) were patterned on MoS_2 followed by etching of MoS_2 channels ($L \approx 0.9$ µm, $W \approx 0.7$ µm) (see Figure S3, Supporting Information). A 30 nm thick Al_2O_3 dielectric layer was then grown by ALD. The top gate word lines (width ≈1.3 µm) were fabricated in the transverse direction to overlap the MoS_2 channels that define the nodes in a 10 × 9 (column, row) crossbar array (**Figure 5**a–d) with the underlying Si substrate serving as a global bottom gate. Additionally, we also fabricated 1 × 9 crossbar arrays for the rapid testing of dual-gated memristors with the same channel dimensions of 0.9 × 0.7 µm^2 (Figure S3, Supporting Information). A histogram from 34 memtransistors shows a mean switching ratio exceeding 10^3 with more than 90% of the devices showing a switching ratio larger than 500 (Figure 5e). While thickness variation in the CVD MoS_2 film (Figure S2b, Supporting Information) can contribute to device-to-device variability, its effect can be mitigated through further optimization of uniformity in MoS_2 monolayer growth.[33]

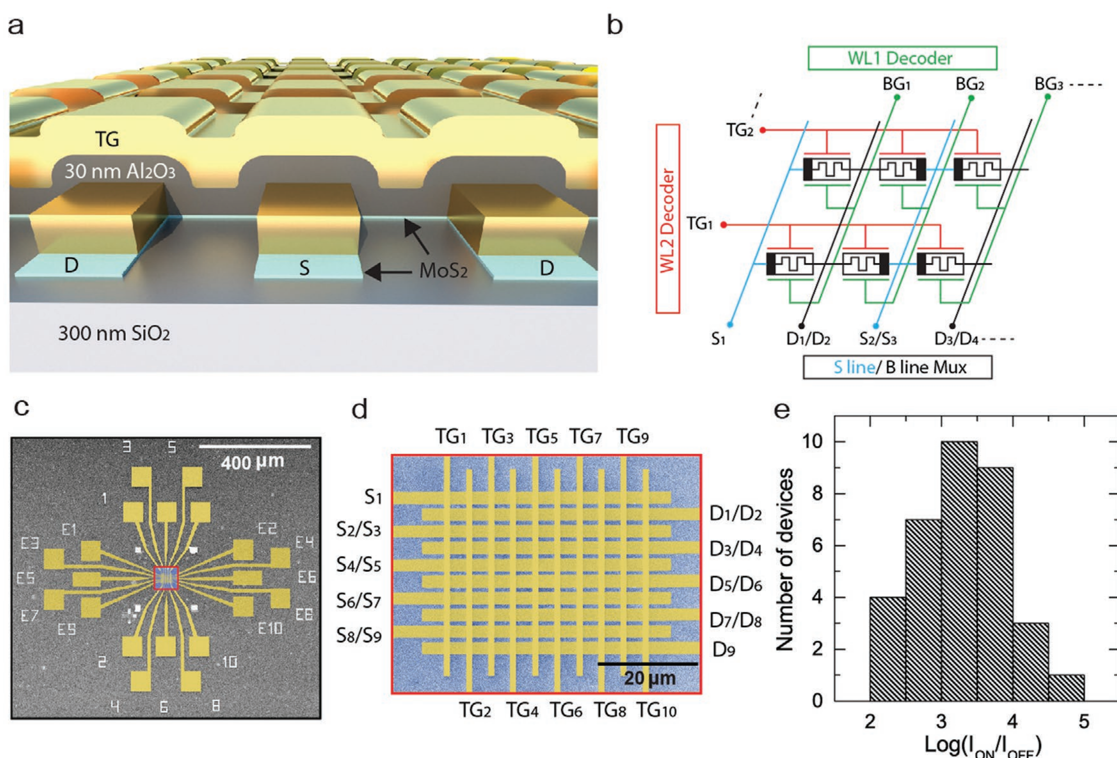

Figure 5. Architecture of the dual-gated MoS_2 memtransistor crossbar array. a) Schematic illustration of a dual-gated MoS_2 memtransistor crossbar array with global silicon bottom gate (word line 1, WL1) and local top gate electrodes (word line 2, WL2) running perpendicular to the drain and source electrodes (bit line B and source line S). b) Diagram of the dual-gated memtransistor crossbar array. The optional local bottom gate electrodes (WL1) are shown to further reduce parasitic capacitance during reading and writing operations. Mux stands for multiplexer. c) False-colored scanning electron microscopy (SEM) image of a 10 × 9 crossbar array. The horizontal electrodes (source and drain) are the alternating B line and S line, and the vertical electrodes (top gate) are WL2. The blue color region indicates the Al_2O_3 oxide layer as the top gate dielectric. d) Zoomed-in SEM image of the active area indicated by the red rectangle in (c). e) Histogram of the switching ratio of 34 MoS_2 memtransistors in 1 × 9 arrays (Figure S3f, Supporting Information) at $V_D = 1$ and $V_{BG} = V_{TG} = 0$ V.

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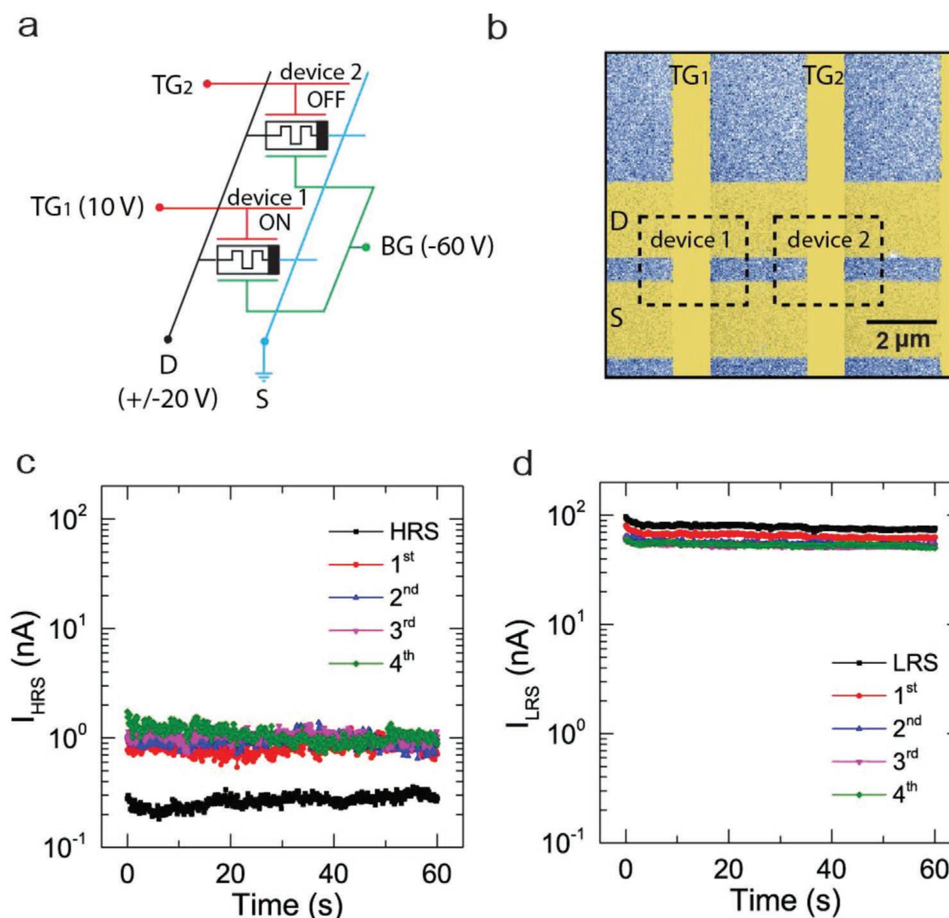

Figure 6. Disturbance test and sneak current characteristics of the dual-gated MoS_2 memtransistor crossbar array. a) Writing operation of device 1 in the crossbar using V_D pulses (1 ms) of 20 and −20 V for switching to HRS and LRS, respectively. All top gate lines except TG_1 (V_{TG1} = 10 V) are floating during writing. For the disturbance test, TG_2 was biased at 10 V and all other TG lines were kept floating. b) False-color SEM image of device 1 and device 2 used in the disturbance test. c,d) Resistance changes of HRS and LRS of the selected device 1 with respect to time (reading conditions, V_D = 1 V, V_{TG1} = 5 V), respectively, after 1st, 2nd, 3rd, and 4th switching events at device 2 (V_{TG2} = 10 V).

A disturbance test of the crossbar array was conducted at V_{BG} = −60 V, which minimizes the read currents in all of the memtransistors (<10 pA, instrument noise floor) except for devices under the selected top gate line (V_{TG} = 10 V). During this test, all other top gate word lines are kept floating. A V_D pulse of 20 or −20 V is then applied to the selected drain bit line to switch the device labeled as "device 1" in **Figure 6** into HRS or LRS, respectively (Figure 6a,b). Even though all memtransistors in the selected bit line receive the same V_D pulse, only device 1 experiences the learning response at V_{BG} = −60 V. This result is confirmed in a subsequent disturbance test where the device labeled as "device 2" in Figure 6 was selected by the top gate word line 2, and HRS and LRS switching was performed by V_D pulses. Following fourfold LRS switching of device 2, HRS of device 1 was again read at a low drain bias (V_D = 1 V), which revealed that the current in HRS was essentially unchanged other than a small initial change in resistance after the first test (Figure 6c). Similarly, LRS of device 1 was also unaffected by HRS switching of device 2 (Figure 6d). The test can be extended to next nearest neighbor devices, which shows a similar relative change in the device current after disturbance pulses even though absolute current values differ from device to device (Figure S11, Supporting Information) Together, these two tests verify that device 1 and device 2 can be written and read independently, and thus dual-gated memtransistors circumvent the sneak current issue of conventional memristor-based crossbar arrays. In summary, the application of V_{BG} = −60 V suppresses the read currents through the field-effect transistor response of the memtransistor without changing the nonvolatile memristive resistance states of the memtransistors in the crossbar array. This isolation of nonvolatile states and read currents without additional elements at each node is the enabling advantage of dual-gated memtransistors for crossbar operation in contrast to conventional memristors or synaptic transistors.[3d]

To highlight broader implications, we compare dual-gated memtransistor crossbar arrays with conventional 1T1M architectures, as outlined in Figure S12 (Supporting Information). The simplest 1T1M architecture has dedicated source lines, bit lines, and word lines for each node (Figure S12a, Supporting Information).[12c] The conventional 1T1M architecture is different from ReRAM passive crossbar arrays (with or without selectors) where voltage and current lines fan-out

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orthogonally.[6b] Alternatively, bit lines can be rotated by 90° to minimize the sneak current in pseudocrossbar arrays (Figure S12b, Supporting Information).[12c] The bit lines can also be shared by neighboring 1T1M nodes to increase areal density (Figure S12c, Supporting Information).[30c] On the other hand, in a M × N dual-gated memtransistor crossbar array, the source line (S_i) and bit line (drain electrode, D_i) can be shared by the neighboring memtransistors in columns i/i+1 and i+1/i+2, respectively, (except when i = 1, M), since neighboring columns can be further isolated by the bottom gate (word line 2) that runs orthogonal to the top gate (word line 1) (Figure 6b; and Figure S12d, Supporting Information). The key novelty is that monolayer MoS_2 memtransistors allow dual gates that can be fabricated on both sides, resulting in the overall bit and source line density being reduced by approximately a factor of two compared to the 1T1M architecture in Figure S12a (Supporting Information).[31b,34]

The scaling argument for conventional two-terminal memristors relies on the nanometer-scale thickness of the vertical channel. In contrast, lateral channels are commonly considered antithetical to similar scaling lengths. However, atomically thin channels allow better electrostatic control compared to bulk semiconductors and in principle nanometer-scale gate lengths are possible.[35] In addition, since the two additional gate lines occupy space in different layers, dual-gating itself is not expected to compromise the scaling limits of 2D materials.[10] Furthermore, dual gates are essential to concurrently achieving tunable learning and low sneak currents. Previous single-gated memtransistors could not achieve both of these functions in crossbar arrays.[8b] Moreover, monolayer MoS_2 can achieve extremely low OFF currents below the instrumentation noise floor, which intrinsically minimizes parasitic power consumption in large crossbar arrays. By employing other best practices from MoS_2 transistors, such as the replacement of metal lines with van der Waals metals or graphene,[10] additional improvements in dual-gated MoS_2 memtransistor performance can be expected as these devices are pushed to their scaling limits. Finally, since the gate lines completely overlap the source and drain electrodes, the leakage current may increase in larger crossbar arrays. However, this issue can be avoided by a simple variation in processing steps. For example, an additional metal-oxide insulation layer can be deposited on top of the source/drain electrodes after the metallization step but before the liftoff step, as has been shown previously in self-aligned heterojunction transistors.[11,36]

5. Artificial Neural Network Demonstration

Finally, we utilize gate tunability to achieve a linear and symmetric synaptic response, which provides clear benefits in the training of ANNs. Training of neural networks based on memristive synapses can be limited by nonlinear and asymmetric learning behaviors despite their relative roles in different learning algorithms.[12,37] In conventional neuromorphic learning algorithms, linear and symmetric weight update rules not only enable higher accuracy in classification tasks, but can also simplify the training process by enabling blind update protocols.[12b,13a,b] Several approaches have been previously employed to improve the linearity and symmetry of two-terminal memristors, including modifying pulse writing schemes in organic electrochemical transistors,[13c] designing multilayer floating gates in MoS_2 synaptic transistors,[38] controlling filament saturation in epitaxial SiGe memristors,[39] and using an additional tunnel barrier or different contact metals in metal-oxide memristors.[13a,b] Broadly, these approaches either modify the device materials in a manner that introduces other device performance tradeoffs or require changes to the pulsing protocol that complicates time-domain multiplexing during training.

In contrast, dual-gated memtransistors improve linearity and symmetry in long-term plasticity via independent access of the gate and drain electrodes during writing and reading operations. To gauge the performance of these devices in network computation, we simulated the supervised learning of a multilayer perceptron (MLP) ANN trained in the recognition of handwritten digits using the MNIST dataset (**Figure 7**a).[40] The first layer of the MLP is composed of an input layer with 28 × 28 (784) input neurons, where each input neuron corresponds to a pixel in the input images. These input neurons are fully connected to the subsequent hidden layer of 300 neurons that utilize a bias neuron and the ReLU activation function. The final layer of ten output neurons (fully connected to this hidden layer) is used to classify each of the ten possible digits in the MNIST data set during training and testing. Training is performed using all 60 000 training images from the MNIST data set for 100 epochs (i.e., 6 million training images) in a randomized order using backpropagation with gradient descent.[41] The recognition rate (i.e., accuracy of classification) is calculated after every epoch of training using all 10 000 testing images from the MNIST data set to assess the performance of the ANN.

In the simulated ANN, the long-term plasticity of dual-gated MoS_2 memtransistors is used to store trained synaptic weights for each layer. The linearity and symmetry of LTP and LTD behavior are improved by dynamic tunability of different learning rates using different V^{W}_{BG} and V^{R}_{BG} pulses (Figure 7b). For example, by writing with $V_D = -15$ V pulses at $V^{W}_{BG} = -20$ V during LTP and with $V_D = 15$ V pulses at $V^{W}_{BG} = 0$ V during LTD, plasticity behavior becomes closer to an ideal linear and symmetric learning rule desired in ANNs (Figure 7b). It should be noted that this linear learning behavior is obtained by tuning only the bottom gate bias, thereby leaving the top gate lines available for node selection during hardware operation. The proposed hardware implementation of the ANN from Figure 7a is outlined in Figure 7c.[39,42] Drain and source electrodes of the memtransistors are used as bit and source lines, forming a crossbar architecture to read the resistance state at each node (via MUX and using V^{R}_{BG} pulse at word line 1). Then, the desired increment in the weight is calculated at each step of training (Figure 7c; and Figure S12d, Supporting Information), and the weight is updated using concurrent V_D and V^{W}_{BG} pulses. Importantly, word line 2 (top gate) allows individual access to memtransistors by minimizing the sneak current. The present MLP uses two memtransistors on neighboring columns in order to achieve positive and negative weight values, similar to previously reported schemes used in conventional memristor crossbars.[37,43] In an ideal case, synaptic weights would be stored and read with complete accuracy. However, practical devices for hardware implementation of synaptic weight storage

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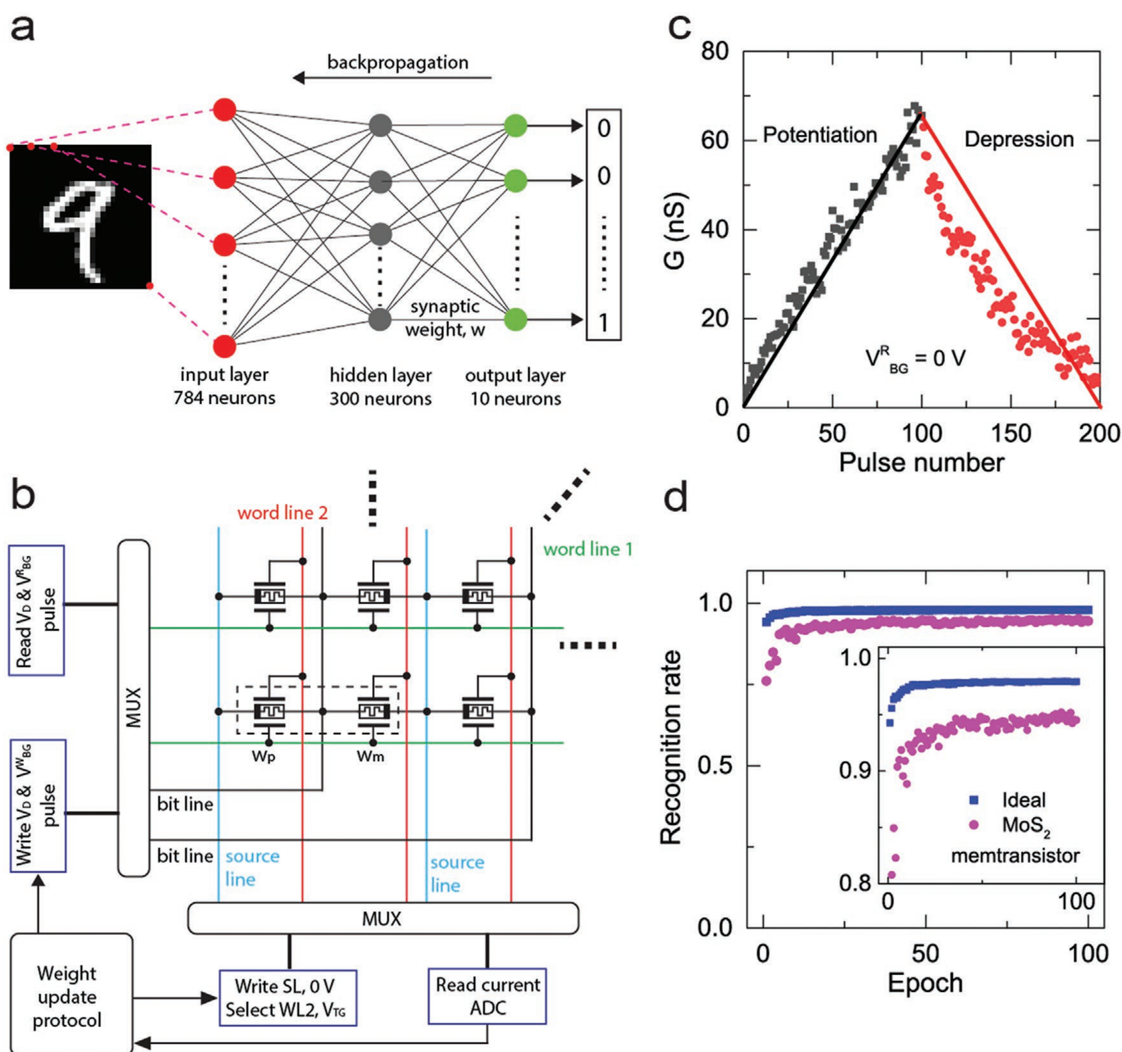

Figure 7. Application of the linear and symmetric synaptic response of dual-gated MoS_2 memtransistors in a simulated ANN. a) The ANN is trained to perform the classification of MNIST handwritten digits using backpropagation. Each input neuron corresponds to a unique pixel in the image. A pair of dual-gated MoS_2 memtransistors was used to represent each synaptic weight (w) between fully connected neurons in the input, hidden, and output layers. b) Circuit block diagram of the hardware implementation of the ANN in a) using dual-gated memtransistor crossbar synapses. The device resistance is read via source lines. Weight updates are accomplished by pulsing bit lines (drain) and word line 1 (bottom gate). Word line 2 (top gate) is used to minimize the sneak current. MUX = multiplexer; ADC = analog-to-digital converter. Two neighboring memtransistors in the dashed box, with conductance levels w_p and w_m, are used to store a synaptic weight, $w = w_p – w_m$. c) Linearity of the LTP and LTD characteristics of a dual-gated memtransistor synapse. The LTP pulsing scheme is $V_D = –15$ V pulses for 1 ms at $V^W_{BG} = –20$ V. The LTD pulsing scheme is $V_D = 15$ V pulses for 1 ms at $V^W_{BG} = 0$ V. The device conductance (G) is read at $V_D = 1$ V and $V^R_{BG} = 0$ V. Solid lines represent ideal linear and symmetric synaptic responses. d) Recognition rate of the simulated ANN using experimental data from (c) achieves an accuracy of 94% in 100 epochs, which is within 3% of the ideal case. The inset shows zoomed in data from the main plot in (d).

present a finite number of conductance states, limiting the precision of stored weight values. A nonideal memtransistor read noise of 10% (Figure 2d) is also simulated during training. Figure 7d shows the performance of an MLP ANN for the ideal case and compares it with the dual-gated MoS_2 memtransistor implementation. The MLP ANN using memtransistors achieves an average recognition rate of 94%, which is only 3% lower than the ideal case. Additionally, our trained MLP ANN using dual-gated MoS_2 memtransistors achieves a recognition rate comparable with the current state-of-the-art, highlighting that the improvements in crossbar architecture do not compromise neuromorphic learning performance.[39]

6. Conclusion

In conclusion, we have introduced dual-gated MoS_2 memtransistors as four-terminal neuromorphic devices that enable gate-tunable learning and efficient integration into crossbar architectures. Small grains in CVD-grown MoS_2 allowed memtransistors with active channel dimensions less than 1 µm and energy consumption per switching cycle as low as 2 pJ. Further reduction in power can likely be achieved with thinner bottom and top gate dielectrics and smaller channel geometries (using smaller grain sizes or patterned lattice defects). The clockwise bipolar resistive switching cycle is explained by the space-charge region near

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the forward-biased contact, as opposed to the reverse-biased Schottky contact that is dominant in single-gated memtransistors. In addition to conventional synaptic transistors,[9d,44] single-gated memtransistors and dual-gated neuristors have also been recently reported in several van der Waals semiconductors and heterojunctions.[9a,c,g,15,45] However, monolayer materials or self-aligned van der Waals heterojunctions would achieve better electrostatic control in dual-gated memtransistors.[11,35,36] As a consequence of this stronger electrostatic control, both LTD and LTP can be modulated as a function of the gate bias during writing, while the output read current can be further controlled by the gate bias without affecting the intrinsic nonvolatile state of the device. This latter effect provides a direct pathway for suppressing sneak currents and crosstalk between nodes in crossbar arrays since all devices except the one being specifically addressed can be placed into an OFF current state without changing their intrinsic memory states. Gate tunability of the learning rate is also exploited to achieve improved linearity and symmetry of the weight update rules, resulting in efficient classification in simulated ANNs. Overall, by providing tunable learning that closely mimics complex biological systems in a manner that is amenable to integration into dense crossbar arrays, dual-gated memtransistors are likely to have broad implications for next-generation neuromorphic computing.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

H.-S.L. and V.K.S. contributed equally to this work. H.-S.L., V.K.S., and M.C.H. conceived the idea and designed the experiments. H.-S.L. and V.K.S. developed the fabrication methods and measured the devices. H.B., H.Y.J., and K.S. conducted growth of MoS_2. W.A.G.R. performed ANN simulations. J.Y. participated in the data analysis. The manuscript was written with contributions of all authors. All authors have approved the final version of the manuscript.

Keywords

2D, artificial neural network, neuromorphic computing, sneak current, synaptic device

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