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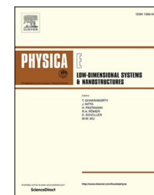

Impact of channel doping engineering on the high-frequency noise performance of junctionless $In_{0.3}Ga_{0.7}As/GaAs$ FET: A numerical simulation study

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ABSTRACT

In this paper, the channel doping engineering is proposed to improve the benchmarking parameters of the analog/radio frequency and the high frequency noise performance of the junctionless (JL)-$In_{0.3}Ga_{0.7}As/GaAs$ device. The proposed structure is called shell doped of channel-JLFET (SDCh-JLFET). The sub-gate doped layer thickness (D) and middle of channel impurity concentration (N_{middle}) are considered as additional factors to improve the analog/radio frequency parameters and high frequency noise performance of device. The SDCh-JLFET with a channel length of 10 nm, D = 1 nm, and $N_{middle} = 2 \times 10^{17} cm^{-3}$ showed the transconductance of G_{mmax} = 3mS/um, unity gain cut-off frequency of f_T = 700 GHz, the minimum noise figure of N_{fmin} = 0.84 db and available associated gain of G_{ass} = 28.5 db. The G_{mmax}, f_T, N_{fmin} and G_{ass} parameters of the SDCh-JLFET device are improved by 76%, 36%, 35% and 26%, respectively, compared to JL-$In_{0.3}Ga_{0.7}As/GaAs$ device without shell doping (JLFET) but with similar dimensions. The SDCh-JLFET device proposed in this paper can be a reasonable candidate for analog/radio frequency applications and high frequency noise.

1. Introduction

In the inversion mode (IM) metal oxide semiconductor field effect transistor (MOSFET), there is an ultra-sharp doping concentration gradient in the source/channel junction and drain/channel junction. Creating source/channel and drain/channel junctions has increased the complexities of fabrication process of the IM transistors in the nanometer regime [1–4]. To solve this problem, for the first time in 2010, the junctionless FET (JLFET) was proposed [4]. In this structure, the source, drain and channel doping were considered to be of the same level and type. Therefore, the fabrication process of JLFET device had less complexity than the IM transistors [1,2,4,5]. Nevertheless, the high channel doping in the JLFET reduces the carrier mobility due to impurity scattering. Thus, the transconductance (G_m) of the JLFET is less than IM device [6,7]. The lower G_m reduces the unity gain cut-off frequency (f_T) of the JLFET. Moreover, scattering due to high impurity concentration in the channel has increased the minimum noise figure (Nf_{min}), noise resistance (R_n) and magnitude of optimum reflection coefficient $|\Gamma_{opt}|$ of the JL device compared to an IM device with similar dimensions [8]. Therefore, the use of the JL device is restricted to analog/radio frequency (RF) applications and high frequency noise applications [8,9].

There are few studies on improving the performance of JL transistors in analog/RF applications and high frequency noise performance [6,7,9,10]. The impact of sidewall spacer layers on the analog/RF performance of the JL double gate silicon transistor was investigated in Ref. [9]. As the spacer dielectric constant increased, G_m and intrinsic gain (A_{V0}) were improved [9]. Moreover, the increase in the spacer dielectric constant reduces f_T and maximum oscillation frequency (f_{max}) [9]. The high frequency noise performance of the nanoscale JL double gate silicon transistor compared to an IM double gate silicon transistor with the same dimensions was investigated in Ref. [8]. The simulation results showed that the impurity scattering of channel in the JLFET reduced the high frequency noise performance compared to the IM device [8]. In a previous paper we reported the JL-$In_XGa_{1-X}As/GaAs$ device to improve

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the benchmarking parameters of analog/RF [10]. By choosing X = 0.3 and thickness of 1 nm for the $In_{0.3}Ga_{0.7}As$ layer, the G_m, A_{V0}, f_T and f_{max} parameters of the JL-$In_{0.3}Ga_{0.7}As$/GaAs device are significantly increased compared to the JL-Si device. In Ref. [10], the high frequency noise performance of the JL-$In_{0.3}Ga_{0.7}As$/GaAs device was neglected.

The main goal of this paper is to study the high frequency noise performance and to improve the benchmarking parameters of analog/RF and high frequency noise of JL-$In_{0.3}Ga_{0.7}As$/GaAs device. In this paper, the shell doped of channel JLFET (SDCh-JLFET) structure is proposed to improve the benchmarking parameters of analog/RF and high frequency noise. In the proposed structure, the sub-gate layer doping in the channel is the same as drain and source doping regions, but is more than the middle of channel doping. In this paper, for the first time, the middle of channel doping concentration (N_{middle}) and thickness of the layer with more doping (D) are considered as additional parameters to improve the high frequency noise performance. The results of the simulations indicate that the choice of shell doped profile in the channel of SDCh-JLFET device improves the electron mobility. As a result, G_{mmax}, f_T and f_{max} are increased compared to the JL-$In_{0.3}Ga_{0.7}As$/GaAs device. The challenges of the fabrication process of the proposed device are also investigated. The simulation results show that the use of lower doping in the GaAs layer in the channel of SDCh-JLFET device reduces N_{fmin} as well as the magnitude of Γ_{opt} in comparison with the devices that have been recently suggested. As a result, the SDCh-JLFET device can be a good candidate for the design of low noise amplifiers (LNAs).

2. Device structure and simulation setup

Fig. 1(a) shows schematic picture of JL-$In_{0.3}Ga_{0.7}As$/GaAs device without shell doping (JLFET) structure and Fig. 1(b) shows the structure of shell doped channel-JLFET (SDCh-JLFET) simulated in this paper. In the simulated structures, to increase gate control over the channel, the double gate technology is used. In the JLFET structure, the source, channel and drain doping are considered the same and of the donor-type (N_D) with the value of $2 \times 10^{19}cm^{-3}$. The channel length, body thickness and gate insulator thickness are 10 nm, 5 nm and 2 nm, respectively. The length of the source and drain is 25 nm Si_3N_4 is considered as the gate insulator. The gate work function is 5.15ev and is obtained by considering p + -polysilicon as the gate electrode [2,11]. The structural parameters of the JLFET device simulated in Fig. 1 (a) are the same as the structural parameters of JL-$In_{0.3}Ga_{0.7}As$/GaAs device proposed in Ref. [10]. In the previous work [10], it was shown that for the $In_{0.3}Ga_{0.7}As$ layer with the thickness of 1 nm and GaAs layer with the thickness of 3 nm in the JL-$In_{0.3}Ga_{0.7}As$/GaAs device, the maximum transconductance (G_{mmax}) was obtained. Therefore, the benchmarking parameters of analog/RF were improved. Thus, in the device of Fig. 1(a), the thickness of the $In_{0.3}Ga_{0.7}As$ and GaAs layers was considered 1 nm and 3 nm, respectively. The device of Fig. 1(b) was proposed to improve the high frequency noise in this paper. The structural parameters of device in Fig. 1(b) were completely similar to those of the device in Fig. 1(a). However, the doping profile of SDCh-JLFET device channel was quite different from the JLFET device. It should be noted that the dopant profiles have a uniform distribution in SDCh-JLFET device. In the channel of device shown in Fig. 1(b), $In_{0.3}Ga_{0.7}As$ layer was considered with high doping concentration and GaAs layer was considered with low doping concentration. In the simulations carried out in this paper, it was assumed that the thickness of the doped layer, D, in the device of Fig. 1 (b) was equal to the thickness of $In_{0.3}Ga_{0.7}As$ layer. In the SDCh-JLFET device, the sub-gate layer doping with thickness D was the same as source/drain doping ($2 \times 10^{19}cm^{-3}$). The GaAS layer doping (N_{middle}) in SDCh-JLFET device was of donor type with the value of $2 \times 10^{17}cm^{-3}$.

In order to simulate the SDCh-JLFET device, the commercial tool was used. The hydrodynamic transport model was considered to determine the electrical characteristics of the proposed structures. In this model, in addition to the drift and diffusion components, the additional current component was considered due to the carrier energy gradient [2,12,13]. The Bohm quantum potential (BQP) model was employed to consider the quantum confinement effect. The BQP model adds a position-dependent quantum potential to the carrier potential energy [2,10,14]. The dependence of mobility on vertical electric field, doping concentration and temperature was considered using Lambardi model [15]. The SRH generation-recombination model, direct generation-recombination model, and non-local band-to-band tunneling were considered to precisely determine the leakage current in the simulated devices [10,16,17]. Given the high doping concentration in the proposed device, the band gap narrowing was used [18]. The energy band model for $In_{0.3}Ga_{0.7}As$ layer was considered based on [19].

The effects of defects and nonsmoothness in the interfacial regions were neglected in our simulations. These effects in real devices flattened the I_D-V_{GS} characteristics because of high electric field effects [20].

3. Results and discussion

The main motivation of this study is to improve the benchmarking parameters of analog/RF frequency and high frequency noise of the proposed device (JL-$In_{0.3}Ga_{0.7}As$/GaAs) in Ref. [10]. Hence, the SDCh-JLFET structure shown in Fig. 1(b) is proposed.

Fig. 2(a) shows I_D-V_{GS} characteristic for the SDCh-JLFET device for different Ds. As can be seen, as D was reduced from 2 nm to 1 nm, the OFF-state current in the SDCh-JLFET device was significantly reduced. In this study, I_D is considered as the OFF-state current for the bias conditions of $V_{GS} = 0$ V and $V_{DS} = 1$ V. The simulation results in the OFF-state show that the sub-gate layer with high doping in the channel of the SDCh-JLFET scan the middle of the channel against the field lines caused by the gate. Therefore, the gate could not properly deplete the middle of the channel. In fact, with a decrease in D, the thickness of the sub-gate layer with high doping is reduced. Therefore, the gate control is

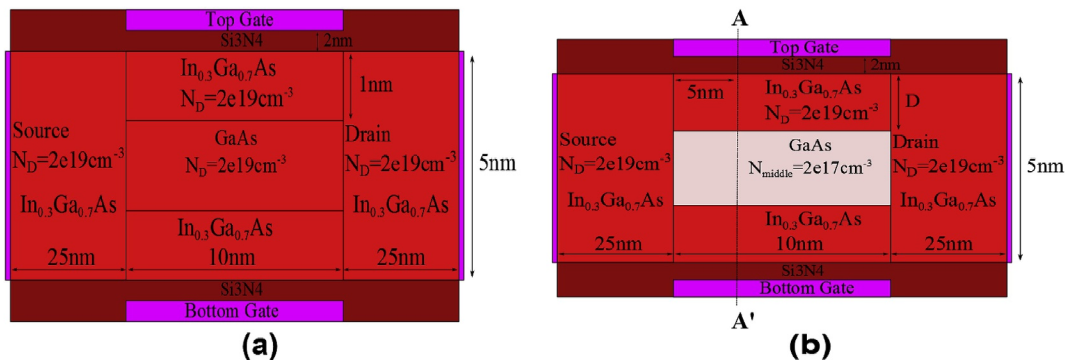

Fig. 1. Schematics (not to scale) of (a) JL-$In_{0.3}Ga_{0.7}As$/GaAs structure and (b) SDCh-JLFET structure simulated in this study. JL-$In_{0.3}Ga_{0.7}As$/GaAs structure is the so-called JLFET. Cutline A-A′ is taken at 5 nm from the source/channel interface towards the channel.

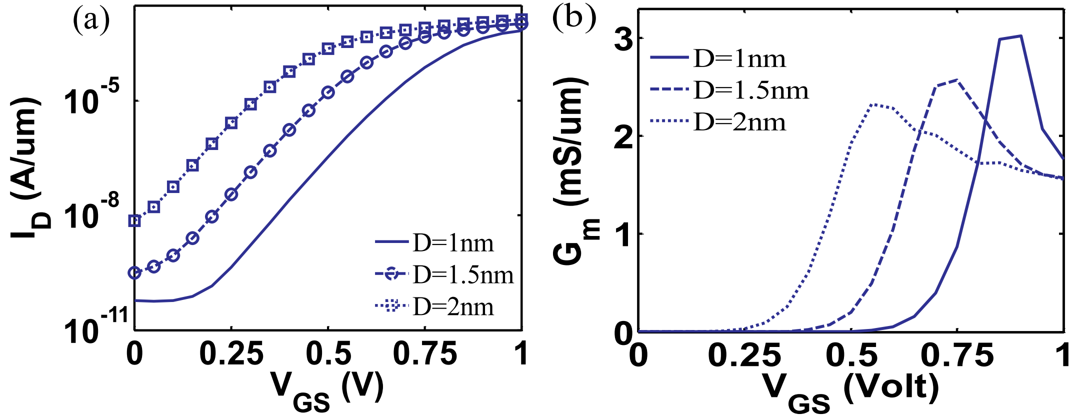

Fig. 2. (a) Transfer characteristics of SDCh-JLFET for various Ds. (b) Transconductance of SDCh-JLFET as a function of V_{GS} for various Ds. Bias condition is $V_{DS} = 1$ V. It should be noted that the maximum transconductance in (b) is considered as G_{mmax}. Structural parameters of simulated devices are noted in section 2.

increased on the middle of the channel. As a result, in the OFF state, the middle of the channel is properly depleted from the electrons and the OFF-state current is considerably reduced.

One of the most important benchmarking parameters in the analog/RF and high frequency noise is transconductance (Gm). Gm represents the ability of the transistor for voltage to current conversion as well as the gate control rate on the channel potential [10,21]. Fig. 2(b) shows $Gm(= \partial I_D/\partial V_{GS})$ for SDCh-JLFET device for various Ds versus V_{GS}.

In this study, the maximum transconductance in Fig. 2(b) is considered as G_{mmax}. Since the series resistance increases by reducing D followed by an increase in the threshold voltage. As a result, the G_{mmax} is distributed at higher gate voltage; see Fig. 2(b). As D was reduced from 2 nm to 1 nm, the Gm in the SDCh-JLFET device was significantly increased. As in Fig. 2(b), for D = 1 nm, D = 1.5 nm and D = 2 nm, G_{mmax} is 3mS/um, 2.5mS/um and 2.3mS/um, respectively, while for the device in Fig. 1(a), $G_{mmax} = 1.7$mS/um [10]. Fig. 3(a) compares the electron mobility along the body thickness of device SDCh-JLFET (A-A′ in Fig. 1(b)) for different Ds in the G_{mmax} bias conditions. In this figure, only half of the body thickness of 5 nm is shown because the electron mobility is identical down to the bottom gate.

According to Fig. 2(b), G_{mmax} occurs for various Ds at different V_{GS}s, but for all the simulated structures in the G_{mmax} bias conditions, $V_{DS} = 1$ V is considered. As represented in Fig. 3(a), the electron mobility in the channel of SDCh-JLFET device increases with a decrease in D. The increased electron mobility with D reduction is noticeable at distances away from the $In_{0.3}Ga_{0.7}As/Si_3N_4$ interface because with the D reduction, the thickness of the region increases with low doping (GaAs layer). As a result, the electron impurity scattering in the GaAs layer is reduced followed by G_{mmax} improvement. Despite the improved G_{mmax} with the D reduction, the ON-state current is distributed at higher gate voltage because the series resistance increases with D reduction and shifts the threshold voltage.

3.1. Challenges for the fabrication process of the proposed device

For the growth of $In_{0.3}Ga_{0.7}As/GaAs$ layers, the molecular beam epitaxy (MBE) method has been proposed [22,23]. One of the challenges for the fabrication is the growth of the Si_3N_4 gate insulator on the $In_{0.3}Ga_{0.7}As$ semiconductor. Using the atomic layer deposition (ALD), the Si_3N_4 gate insulator on the $In_{0.3}Ga_{0.7}As$ semiconductor can be made with acceptable quality [24]. In order to make side contacted source/-drain, the double trench method was proposed [25]. The main challenge in the fabrication process of the SDCh-JLFET device is the precise control of shell doping. In order to dope the surface areas of the channel, the level of 2×10^{19}cm^{-3}, D thickness, monolayer doping (MLD) and microwave annealing (MWA) were proposed [26,27]. The simulation results showed that SDCh-JLFET device proposed in Fig. 1(b) worked as junctionless transistors in the depletion mode. Therefore, the proposed device could be classified as a junctionless transistor.

3.2. Choosing an optimum amount for middle of channel doping and sub-gate doped layer thickness

Fig. 3(b) shows the G_{mmax} value as a function of middle of channel

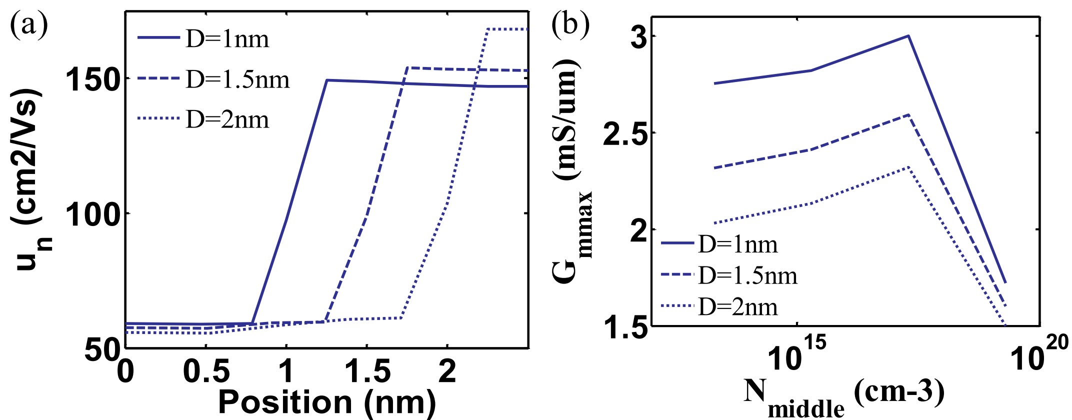

Fig. 3. (a) Electron mobility (μ_n) along the body thickness (A-A′ in Fig. 1(b)) for various Ds in G_{mmax} bias condition. Due to symmetry, only half of the body thickness is depicted. (b) G_{mmax} as a function of N_{middle} for various Ds. In (b), the bias value of V_{GS} in G_{mmax} has been varied for various Ds, but the bias value of V_{DS} is equal to 1 V.

doping (N_{middle}) for various Ds. The results of our simulations indicate that, for various Ds, the bias value of V_{GS} in G_{mmax} varied [10]. As seen in Fig. 3(b), the maximum G_{mmax} for a certain D is obtained at $N_{middle=}2 \times 10^{17}cm^{-3}$. The simulation results show that, with an increase in N_{middle}, the height of the potential barrier against the electron is reduced in the source/channel interface ($In_{0.3}Ga_{0.7}As$/GaAs interface) because, as N_{middle} increases, the impurity concentration in the GaAs layer approaches the impurity concentration in the source region. As a result, the electron density injected from the source to the GaAs layer increases in the channel (see Fig. 4(a)). It can be said that an increase in electron density with increased N_{middle} could raise the channel conduction. Fig. 4(b) shows the electron mobility in the G_{mmax} bias conditions along the device for different N_{middle} values. As can be observed, with the increase in N_{middle}, the electron mobility is reduced because the increased N_{middle} can raise impurity scattering. In fact, with increase in N_{middle}, the positive and negative factors competed to determine G_{mmax}. An increase in N_{middle} up to $2 \times 10^{17}cm^{-3}$ increases the channel conduction and plays an important role in increasing G_{mmax} as a positive factor. The increase in N_{middle} to a value larger than $2 \times 10^{17}cm^{-3}$ increases the electron scattering in the channel and decreases G_{mmax} as a negative factor. Fig. 3(b) shows that, with a decrease in the thickness of doped layer at certain N_{middle}, the G_{mmax} is improved because, with the D reduction, the thickness of the layer with lower doping (GaAs) is increased in the channel. As a result, the improved electron mobility in GaAs layer improves the G_{mmax}.

3.3. Benchmarking parameters

In this section, the effect of doped layer thickness on the benchmarking parameters of the analog/RF of the proposed device in Fig. 1(b) is investigated, and the results are compared with the results of the device reported in Ref. [10].

The intrinsic gain of a device, A_{V0}, is the product of the G_m in the output resistance (R_0) [10,21]. Fig. 5(a) shows the intrinsic gain of SDCh-JLFET device versus V_{GS} for various Ds and $N_{middle=}2 \times 10^{17}cm^{-3}$, in $V_{DS} = 1$ V. As can be seen, for the above threshold region, the intrinsic gain of the SDCh-JLFET device with D = 1 nm is higher than SDCh-JLFET device with D = 2 nm and D = 1.5 nm. The results of our simulations show that, with an increase in gate voltage, the output resistance of the simulated devices is reduced because, with an increase in the gate voltage, the sub-gate depletion layer width is reduced and increased the cross-section of current in the channel. Furthermore, based on the simulations carried out in this paper, the I_D-V_{DS} curve slope of SDCh-JLFET device with D = 1 nm is less than that of the simulated devices. As a result, its output resistance is greater. The increased output resistance of SDCh-JLFET with D = 1 nm as well as its increased transconductance raises the maximum intrinsic gain of the SDCh-JLFET device with D = 1 nm. The simulation results show that the maximum intrinsic gain of the SDCh-JLFET device with D = 1 nm is 34 db, while the maximum intrinsic gain reported for the device in Fig. 1(a) is 32.5 db [10]. This is due to the fact that transconductance and output resistance of SDCh-JLFET with D = 1 nm are higher than those of JL-FET.

Fig. 5(b) shows the total gate-to-gate capacitance of the simulated structures for $V_{DS} = 1$ V. Note that C_{GG} of simulated structures has been calculated based on the method discussed in Ref. [10]. In this method to calculate C_{GG}, it is assumed that $V_{DS} = 1$ V and gate voltage ranged from 0 V to 1 V swept at 1 MHz frequency. As shown in Fig. 5(b), with the increase in the gate voltage, the C_{GG} increases. As the gate voltage increases, the cross-section of current in the channel is increased. Therefore, the sub-gate depletion layer width is reduced in the simulated devices followed by an increase in C_{GG}. Fig. 5(b) also shows that, for a certain value of V_{GS} with D reduction in the subthreshold region, the C_{GG} is reduced and, in the above threshold region, C_{GG} is increased. Based on the simulation results performed in this study, in the SDCh-JLFET device with D = 1 nm, the width of the sub-gate depletion layer in the subthreshold region is higher than the devices simulated by D = 1.5 nm and D = 2 nm. As a result, the C_{GG} of SDCh-JLFET device with D = 1 nm is less than the devices simulated by D = 1.5 nm and D = 2 nm. The simulation results also show that, in the above threshold region, the electron in the channel moves from the path with less resistance. Therefore, with the D reduction, the distance between electron in the channel and gate is reduced. Therefore, the maximum C_{GG} increases.

One of the other benchmarking parameters in the analog/RF is the unity gain cut-off frequency, f_T, which is defined as [10]:

$$f_T = \frac{G_m}{2\pi C_{gg}} \tag{1}$$

Fig. 6(a) shows the unity gain cut-off frequency of the simulated structures versus V_{GS} at $V_{DS} = 1$ V. As can be seen, the maximum unity gain cut-off frequency (f_{Tmax}) increased with D reduction. In fact, the improvement in the G_{mmax} of SDCh-JLFET device with D = 1 nm has compensated for the increase in C_{GG} in the above threshold region and increases the f_{Tmax} of SDCh-JLFET device with D = 1 nm as compared to SDCh-JLFET devices with D = 1.5 nm and D = 2 nm. The f_{Tmax} of SDCh-JLFET device with D = 1 nm is 700 GHz, which is significantly improved compared to f_{Tmax} of JLFET device in Fig. 1(a), $f_{Tmax} = 513$ GHz [10]. The maximum oscillation frequency (f_{max}) of a transistor is discovered when unilateral power gain equal to 1 [10]. The simulation results show that the SDCh-JLFET device with D = 1 nm indicates $f_{max} = 2150$ GHz, see Fig. 6(b), while for the JLFET device in Fig. 1(a), $f_{max} = 1720$ GHz [10]. In fact, the improved G_m in SDCh-JLFET device with D = 1 nm significantly improves f_{Tmax} as well as f_{max} compared to JLFET device [10].

According to the above results, in the rest of this study, the optimum

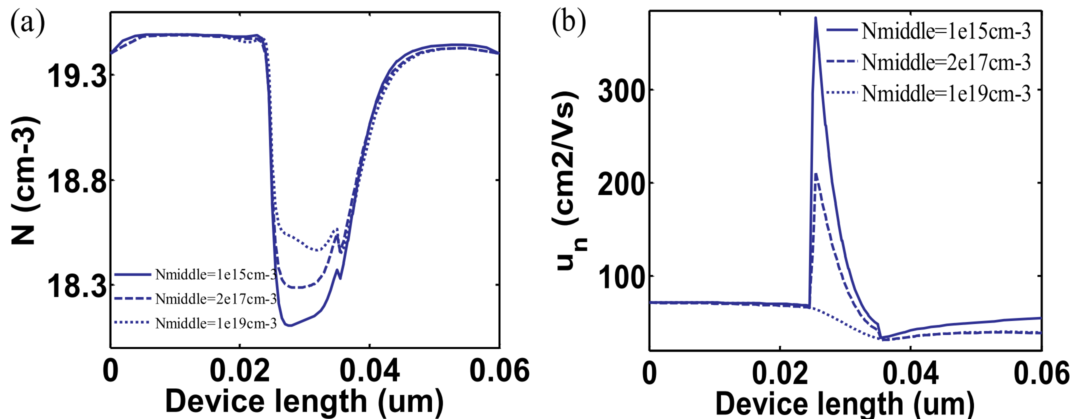

Fig. 4. (a) Electron density and (b) electron mobility taken horizontally across the simulated SDCh-JLFET structures, for 2.5 nm from the surface. Simulation is performed for the G_{mmax} bias condition.

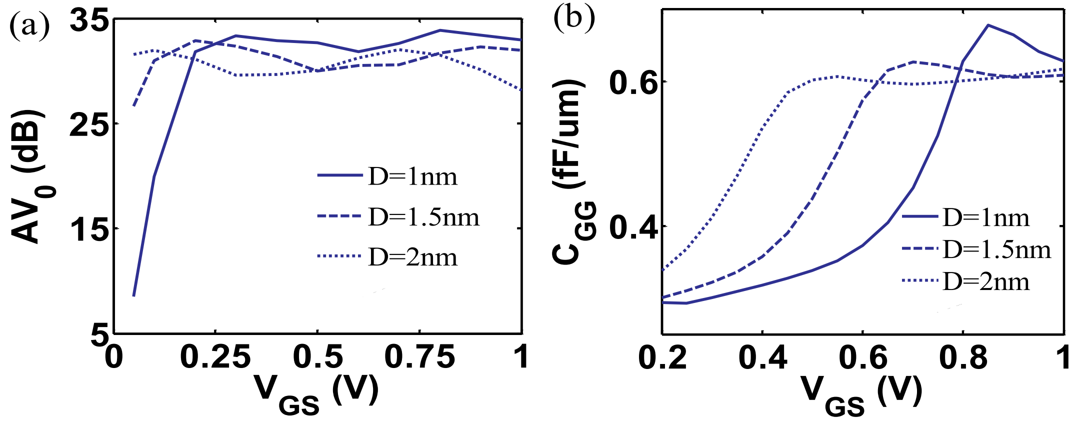

Fig. 5. (a) Intrinsic gain and (b) total gate-to-gate capacitance as a function of V_{GS} in $V_{DS} = 1$ V for various Ds in SDCh-JLFET structure.

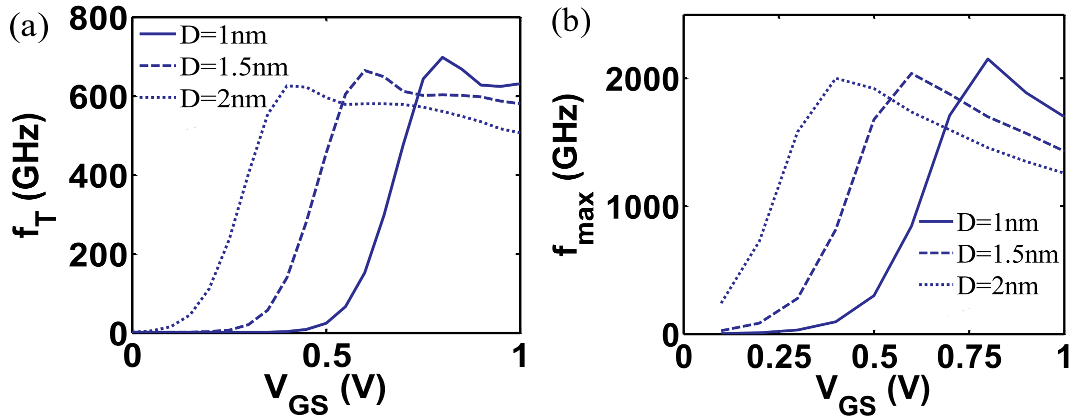

Fig. 6. (a) f_T and (b) f_{max} as a function of V_{GS} in $V_{DS} = 1$ V for various Ds in SDCh-JLFET structure.

thickness of the doped layer is selected 1 nm.

3.4. High frequency noise performance

The random oscillations of current and voltage in the terminals of a device would cause noise. According to the Drude model, the noise at the terminal of a device is due to the time-dependent oscillations in the electron density and drift velocity [28].

In this study, the gate current oscillation spectrum density (S_{Ig}), drain current oscillation spectrum density (S_{Id}) as well as their cross-correlation (S_{IgId}) are calculated with the two-dimensional noise simulator [28]. To evaluate the high frequency noise performance of the proposed devices, the Pucel's model has been used [8,29–31]. The benchmarking parameters of high frequency noise in the field effect devices include minimum noise figure (Nf_{min}), equivalent resistance noise (R_n), amplitude and phase of optimal reflection coefficient (Γ_{opt}) and available gain (G_{ass}). To investigate the benchmarking parameters of the high frequency noise, it is necessary to calculate the noise normalized parameters [8,29–31]. The noise normalized parameters based on the Pucel's model are P, R and C. P refers noise at drain terminal, R refers to noise at gate terminal and C refers to normalized correlation coefficient between the noise resources of the drain and gate current. The normalized noise parameters are calculated from the following equations [8,29–31]:

$$P = \frac{S_{Id}}{4K_BT|Y_{21}|}$$
$$R = \frac{S_{Ig}|Y_{21}|}{4K_BT|Y_{11}|^2} \qquad (2)$$
$$C = \frac{\mathrm{Im}[S_{IgId}]}{\sqrt{S_{Ig}S_{Id}}}$$

where K_B is the Boltzmann's constant and T is temperature per Kelvin. Y_{21} and Y_{11} are the short-circuit admittance parameters of the simulated device. Fig. 7(a), (b) and (c) are respectively comparing P, R and C of the SDCh-JLFET device and JLFET device shown in Fig. 1(a). As demonstrated, in most parts of the shown diagrams, P and R of the SDCh-JLFET device are less than JLFET because the electron mobility in the GaAs region with low doping in SDCh-JLFET is more than JLFET device shown in Fig. 1(a). It can be said that the reduced electron scattering in the channel of SDCh-JLFET device reduces the noise measured at the gate and drain terminals in comparison with JLFET device. Fig. 7 (c) shows that C of SDCh-JLFET device is lower than JLFET reported in Ref. [10], in most parts of the diagram. Equation (2) confirms the results of Fig. 7 (c).where K_B is the Boltzmann's constant and T is temperature per Kelvin. Y_{21} and Y_{11} are the short-circuit admittance parameters of the simulated device. Fig 7(a)–(c) are respectively comparing P, R and C of the SDCh-JLFET device and JLFET device shown in Fig. 1(a). As demonstrated, in most parts of the shown diagrams, P and R of the SDCh-JLFET device are less than JLFET because the electron mobility in the GaAs region with low doping in SDCh-JLFET is more than JLFET device shown in Fig. 1(a). It can be said that the reduced electron scattering in the channel of SDCh-JLFET device reduces the noise

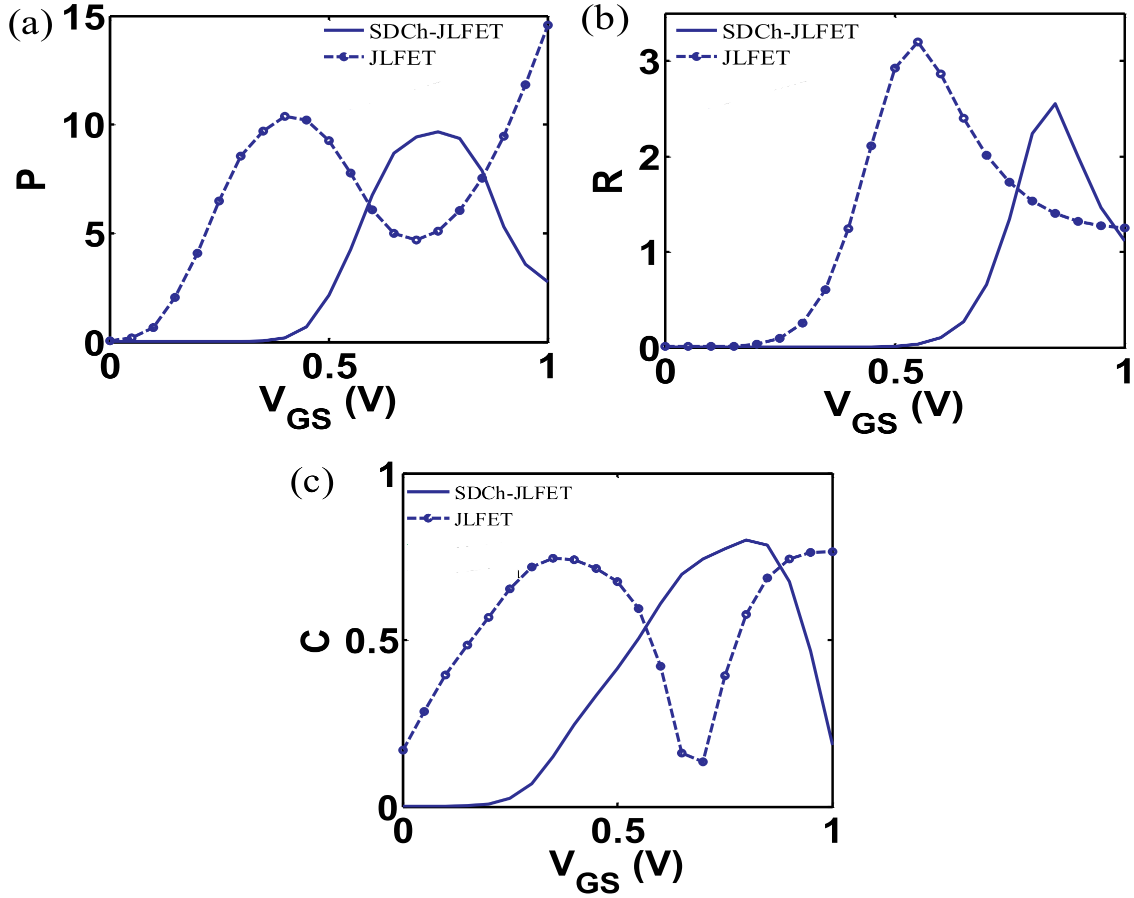

Fig. 7. Extraction of (a) P, (b) R and (c) C as a function of V_{GS} in $V_{DS} = 1$ V for both SDCh-JLFET and JL-FET structures shown in Fig. 1.

measured at the gate and drain terminals in comparison with JLFET device. Fig. 7 (c) shows that C of SDCh-JLFET device is lower than JLFET reported in Ref. [10], in most parts of the diagram. Equation (2) confirms the results of Fig. 7 (c). The benchmarking parameters of the high frequency noise of the field effect devices can be calculated from the following equations [8,29–31]:

$$Nf_{\min} = 1 + 2f \Big/ f_t \sqrt{PR(1 - C^2)}$$
$$G_{ass} = \frac{f_t}{f} \frac{\sqrt{1 - C^2}}{C} \frac{(C_{gs} + C_{gd})}{C_{gd}} \tag{3}$$
$$R_n = \frac{P}{g_m}$$
$$\Gamma_{opt} = \frac{1 - Y_{opt}}{1 + Y_{opt}}$$

where Y_{opt} is the normalized optimum noise source admittance. The gate width for the simulated structures is considered 100 µm [8]. In this study, the benchmarking parameters of the high noise frequency at f = 40 GHz per V_{GS} are extracted according to Equation (3) [8]. The corresponding gate bias with the minimum amount of N_{fmin} is particularly important in the design of LNAs [8,30,31]. N_{fmin} for SDCh-JLFET and JLFET devices simulated in this study is minimized at $V_{GS} = 1$ V and $V_{GS} = 0.8$ V, respectively. Then, in the gate bias corresponding to the minimum amount of N_{fmin}, for SDCh-JLFET and JLFET devices, the frequency analysis is performed. The benchmarking parameters of high frequency noise per frequency are shown in Fig. 8. As in Fig. 8(a), N_{fmin} of the SDCh-JLFET device is significantly reduced compared to JLFET device. A decrease in N_{fmin} of SDCh-JLFET device compared to JLFET device, in addition to improvement in P, R and C parameters, can be attributed to an increase in f_T. From a physical point of view, the electron scattering in the middle of channel of SDCh-JLFET device compared to the JLFET device improves N_{fmin}. Fig. 8(b) compares the available associated gain, G_{ass}, for the simulated devices. To calculate G_{ass}, the C_{gs}/C_{gd} ratio per frequency is extracted. The results of our simulations show that C_{gs}/C_{gd} ratio of SDCh-JLFET device is slightly higher than JLFET device. The improved G_{ass} of SDCh-JLFET device compared to JLFET can be due to the improved C_{gs}/C_{gd} ratio in addition to improved f_T of SDCh-JLFET device. The improved G_{ass} in SDCh-JLFET device in comparison to JLFET, in addition to the improved f_T of SDCh-JLFET device, can be attributed to the improved C_{gs}/C_{gd} ratio. Noise resistance, R_n, measures the sensitivity of N_{fmin} to changes in impedance or admittance of the source. As a result, one of the most important noise parameters is high frequency noise [8].

Fig. 8(c) compares the R_n in the simulated devices. As seen, R_n in the SDCh-JLFET device is less than JLFET device because G_m of SDCh-JLFET device is higher than JLFET. The lower R_n refers to the wider match bandwidth in the minimum N_{fmin} status. One of the other important parameters in the high frequency noise performance is Γ_{opt}. Smaller Γ_{opt} means easier design of the matching networks at the input of transistor for the LNA in the minimum N_{fmin} status [8,31]. To extract Γ_{opt}, the Y_{opt} should be determined (see Equation (3)). We extracted Y_{opt} based on the equations expressed in Refs. [31–33]. Fig. 8(d) compares the magnitude and phase of Γ_{opt} for simulated devices. As seen, the magnitude of Γ_{opt} of SDCh-JLFET device is less than JLFET. Based on the equations expressed in Refs. [31,33], the larger f_T reduces Y_{opt} followed by the decreases magnitude of Γ_{opt}. Therefore, it can be said that the larger f_T of SDCh-JLFET device reduces magnitude of Γ_{opt} compared to JLFET.

The SDCh-JLFET device proposed in this study with the channel length of 30 nm had $f_{Tmax} = 310$ GHz and $G_{mmax} = 2.4$mS/um. The

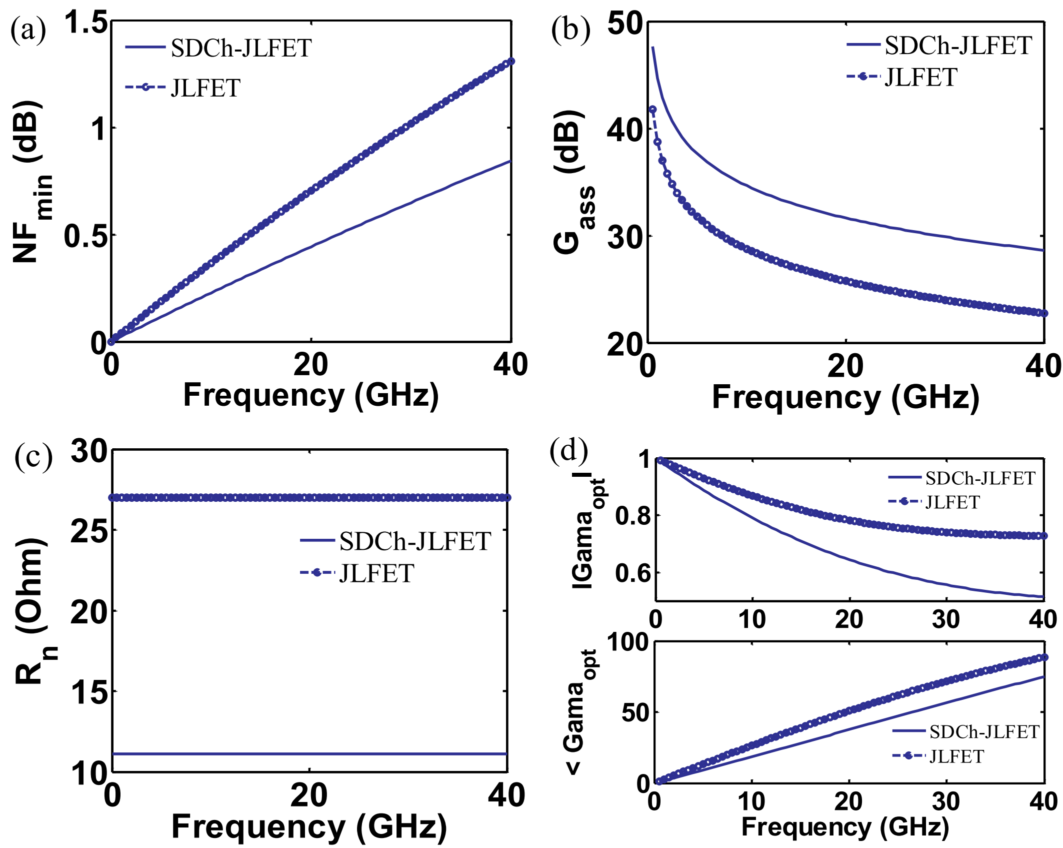

Fig. 8. Extraction of (a) Nfmin, (b) Gass, (c) Rn and (d) magnitude ($|Gama_{opt}|$) and phase ($<Gama_{opt}$) of Γ_{opt} versus frequency for both SDCh-JLFET and JL-FET structures shown in Fig. 1. The bias conditions are $V_{GS} = 1$ V and $V_{DS} = 1$ V for SDCh-JLFET. The bias conditions are $V_{GS} = 0.8$ V and $V_{DS} = 1$ V for JLFET.

underlap double gate junctionless transistor (DGJLT) device proposed in Ref. [9] with the channel length of 30 nm had $f_{Tmax} = 175$ GHz and $G_{mmax} = 1.5$mS/um.The dopingless tunnel field effect transistor (DL-TDET) device proposed in Ref. [34] with the channel length of 30 nm had $f_{Tmax} = 5$ GHz and Gmmax = 12μS/um. The double gate junctionless MOSFET device proposed in Ref. [8] with the channel length of 30 nm at f = 40 GHz had $Nf_{min=}1.1$ dB, $R_n = 34$ Ohm and $G_{ass} = 15$ dB. The SDCh-JLFET proposed in this paper with the channel length of 30 nm at f = 40 GHz had $R_n = 9.16$ Ohm, $Nf_{min} = 0.78$ dB and $G_{ass} = 18.9$ dB.

The above results showed the superiority of SDCh-JLFET structure proposed in this paper to the structures proposed in Refs. [8,9,34]. As a result, the SDCh-JLFET structure proposed in this paper can be a proper candidate for analog/radio frequency applications and high frequency noise.

4. Conclusion

In this paper, the improvement of the benchmarking parameters of analog/radio frequency and high frequency noise performance of JL-$In_{0.3}Ga_{0.7}As$/GaAs device was investigated. The impurity concentration of the sub-gate layer in the channel of the proposed device is the same as the impurity concentration of source and drain regions, but more than the impurity concentration of the channel. The use of shell doping profile in the SDCh-JLFET device increases the electron mobility in the channel; therefore, G_{mmax} is increased. As middle of channel doping concentration increases, the increased electron density in the channel as a positive factor and reduced electron mobility as a negative factor are competing to determine G_{mmax}. The results of the simulations show that, for $N_{middle} = 2 \times 10^{17} cm^{-3}$ and D = 1 nm, the highest G_{mmax} is achieved. f_T of the proposed structure is higher than that of the JL-$In_{0.3}Ga_{0.7}As$/GaAs structure without shell doping. As a result, Nf_{min} and G_{ass} of the proposed structure compared to the JL-$In_{0.3}Ga_{0.7}As$/GaAs structure are increased by 36% and 25%, respectively. The numerical simulations show that, at frequency f = 40 GHz, the noise resistance of SDCh-JLFET and JLFET devices are 11.1Ω and 27Ω, respectively. Thus, in the minimum Nf_{min} status, the match bandwidth of SDCh-JLFET device is wider than the JLFET device. The proposed SDCh-JLFET device can be a proper candidate to be used in low noise Amplifiers.

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