FPGA IMPLEMENTATION GUIDE

MIMO-OFDM Underwater Acoustic Communication System

From Simulink Modeling to HDL Deployment

125 kHz Center Frequency

Zynq FPGA Platform

2×2 MIMO Support

Technical Implementation Document

2025

IMPLEMENTATION ROADMAP

From Theory to Deployment

01 System Architecture

Foundation specifications, hardware platform, and PS/PL partitioning strategy.

125 kHz Center · 10 kHz Bandwidth · K=1024 · 500 kHz Sampling

02 Simulink Modeling

Baseband TX/RX chain development with HDL-compatible fixed-point design.

QPSK Mapping · Differential Encoding · IFFT/FFT · CP Insertion/Removal

03 FPGA HDL Design

HDL Coder implementation, AXI interfaces, and Vivado integration.

AXI4-Stream · AXI4-Lite · DMA · Timing Closure · Resource Optimization

04 PS Integration

ARM software drivers, DMA control, and validation methodology.

DMA · Doppler Resampling · Beta Algorithm · BER/MSE Metrics

05 MIMO Extension

2×2 diversity combining and spatial multiplexing roadmap.

Diversity Combining · SNR Weighting · Spatial Multiplexing · ZF/MMSE

06 Deliverables

Complete implementation package and common pitfalls.

Simulink Models · HDL Cores · Vivado Design · Test Reports

01

System Architecture

Foundation specifications, hardware platform, and PS/PL partitioning strategy

SYSTEM SPECIFICATIONS

Hardware Platform & Parameters

Signal Parameters

Center Frequency	125 kHz
Bandwidth	10 kHz
Subcarriers (K)	1024
Subcarrier Spacing	~9.7656 Hz
Symbol Time	~102.4 ms
Cyclic Prefix	25 ms (250 samples)

Detection Method

Frequency-domain differential encoding with differentially coherent detection to avoid explicit channel estimation. Doppler handling through coarse resampling at frame level with block-level residual correction.

$$X_k = S_k \cdot X_{k-1}$$

Hardware Platform

FPGA

MicroZed (XC7Z020) - Zynq-7000 SoC

DAC

LTC1668 (16-bit, 50 Msps)

ADC

LTC1740 (14-bit, ≤6 Msps)

Transducers

TC4013 (Transmit/Receive)

Amplifiers

ZHL-6A+ PA, VP2000 Preamp

Sample Rate

500 kHz (baseband complex)

PS/PL Partitioning

PL (FPGA)

OFDM PHY datapath, IFFT/FFT, CP, sync correlator, stream I/O, timing control

PS (ARM)

Framing, control, AXI DMA setup, Doppler resampling, logging, MAC

SYSTEM ARCHITECTURE

OFDM Signal Chain Architecture

↑ TX Signal Chain (Transmit Path)

↓ RX Signal Chain (Receive Path)

Sample Rate Conversion

10 kHz baseband ↔ 500 kHz passband via L/M=50 polyphase FIR filters

AXI4-Stream

32-bit I/Q (16-bit each) with TLAST, TVALID/TREADY handshaking

AXI4-Lite Control

NCO, CP length, resampler ratio, sync threshold, Beta parameters

02

Simulink Baseband Modeling

Step-by-step Simulink model development and validation

SIMULINK MODELING · TRANSMITTER

TX IP Configuration

1 Bit Source & Framing

Frame structure: 2 preamble symbols + 8 data blocks

P1 + P2 + Block1...Block8

2 QPSK Mapper

Gray-coded constellation mapping to fixed-point

Modulation	Format
QPSK	s16.14

3 Differential Encoder

Frequency-domain differential encoding per active bin

$X_k \leftarrow S_k \cdot X_{k-1}, X_0 = 1+j0$

4 Subcarrier Mask & Pilots

Active bins 49–975, pilots every 16th bin

Active	Pilots	Data
~927	~58	~869

5 IFFT 1024

Streaming radix-2 IFFT with natural order output

Size	Scaling
1024	$1/\sqrt{K}$

6 Windowing & CP Insertion

Raised cosine 10% taper, append 250-sample CP

Window	CP
10% RC	250

7 Interpolation (L=50)

Polyphase FIR upsampler from 10 kHz to 500 kHz

Factor	Passband	Stopband
50	12 kHz	≥70 dB

8 Digital Upconversion

Complex NCO mixer to 125 kHz IF with bandpass FIR

NCO	Output
125 kHz	500 kHz

SIMULINK MODELING · RECEIVER

RX IP Configuration

1 AXI4-Stream Input

32-bit I/Q from ADC via DMA

Width	Rate
32-bit	500 kHz

2 Digital Downconversion

Complex mixer at 125 kHz with LPF

NCO	LPF
-125 kHz	12 kHz

3 Decimation (M=50)

Polyphase FIR decimator to 10 kHz baseband

Factor	Output
50	10 kHz

4 Preamble Correlator

Complex correlation for frame sync

Outputs: Start index, delay, bulk Doppler

5 Coarse Doppler Resampler

Variable-rate polyphase resampler

Ratio: Q16.16 from PS based on preamble

6 CP Removal & FFT

Drop 250 samples, 1024-pt FFT

CP	FFT
250	1024

7 Beta Algorithm (Rotator)

Residual Doppler correction per block

$$Y_k \rightarrow Y_k \cdot e^{-j2\pi k\varepsilon}$$

8 Differential Detector

Multiply by conjugate to avoid division

$$Z_k = Y_k \cdot Y_{k-1}^*$$

9 QPSK Slicer & Metrics

Hard-decision with BER/MSE accumulation

Decision	Metrics
Hard	BER/MSE

03

FPGA-Ready HDL Design

From Simulink to synthesizable HDL with timing closure

FPGA IMPLEMENTATION

HDL Coder Implementation Strategy

Design Methodology

- **Single-Rate Streaming**
  One sample per clock with explicit valid/ready handshaking
- **Fixed-Point Word Lengths**
  s18.16 baseline, s20.18 around mixers/FFT, s24.20 optional
- **Vendor FFT IP**
  Xilinx FFT IP or HDL-optimized Simulink FFT for timing closure
- **Resource Sharing**
  Multipliers shared in differential encoder, pipelined complex operations
- **AXI Interfaces**
  AXI4-Stream for data, AXI4-Lite for control registers

Timing Constraints

PL Clock Frequency	**100–150 MHz**
Sample Clock (500 kHz)	**Easy closure**
Baseband Clock (10 kHz)	**Relaxed timing**
Pipeline Stages	**Multi-cycle**

AXI4-Stream Endpoints

TDATA Format

I[15:0] | Q[15:0] (32-bit)

Handshaking

TVALID/TREADY with TLAST at end-of-frame

Backpressure

Ready/valid handshake prevents underflow at block level

AXI4-Lite Control Registers

0x00: NCO Freq Q16.16 ratio	**0x04: CP Length** Samples
0x08: Bin Mask Ptr DDR address	**0x0C: Pilot Spacing** Bins
0x10: Resampler Ratio Q16.16	**0x14: Sync Threshold** Q1.15
0x18: Beta Count Candidates	**0x1C: Epsilon Select** Q2.30

FPGA INTEGRATION

AXI Interface Mapping & Vivado Integration

AXI4-Stream Protocol

TDATA Signal Structure

I Component	Q Component
Bits 15:0	**Bits 31:16**

Control Signals

TVALID	**Data valid indicator**
TREADY	**Ready to accept**
TLAST	**End-of-frame marker**
TKEEP	**Full width (all bytes valid)**

Throughput: Continuous streaming at 500 kHz sample rate with backpressure

DMA Engine Configuration

- **Large Burst Transfers**
  Maximize throughput, minimize overhead
- **Scatter-Gather**
  Continuous streaming with ring buffers
- **Frame Buffering**
  Ring buffers in DDR for TX and RX frames

Vivado Block Design

Clocking Architecture

PL clocks at 100-150 MHz with separate domain for FFT

Main PL	Sample
100-150 MHz	**500 kHz**

AXI Interconnect

SmartConnect for memory-mapped peripherals with non-overlapping decode ranges

Clock Domain Crossing

CDC FIFOs where domains cross with handshake synchronization

I/O Interfaces

DAC Interface

Parallel LVDS or SPI with packer for I/Q samples

ADC Interface

Parallel LVDS or SPI with frame alignment

Clock Sharing

Reference clock between TX/RX to reduce CFO

04

PS Integration & Testing

Software drivers, DMA control, and validation methodology

SOFTWARE INTEGRATION

PS Software Architecture & Testing Sequence

PS Software Responsibilities

1. **AXI DMA Setup**
   Continuous TX/RX with ring buffers, interrupt or polling
2. **Frame Building**
   Compose preamble + 8 blocks, map payload bits, program PL registers
3. **Coarse Doppler Resampling**
   Estimate bulk scaling from preamble, adjust resampler ratio
4. **Beta Algorithm**
   Per-block residual Doppler correction via pilot hypothesis testing
5. **Metrics & Logging**
   Collect FFT outputs or decisions, compute BER/MSE on PS

Testing & Validation Sequence

1. Digital Loopback

AXI-S TX→RX direct internal path. **Expected:** BER≈0, validate TLAST and no stalls

2. Cable/DAC→ADC Loopback

Through DAC→ADC path with attenuators. **Check:** NCO alignment, preamble sync, CP alignment

3. Near-Field Acoustic

Short-range tank with low gain. **Verify:** Sync and symbol decisions at nominal SNR

4. Tank Tests (Single-Antenna)

Measure multipath vs CP, enable windowing, record BER/MSE/BLER

5. MIMO Diversity

Calibrate phase/gain, enable combiner, compare best-antenna vs weighted combining

6. Doppler Robustness

Introduce motion, tune coarse resampling, enable Beta per block

Minimal PS C Application

Initialization: Configure TX/RX IP registers (NCO, CP, pilot spacing)

DMA Setup: SimpleTransfer for TX and RX buffers

Main Loop: Wait for completion, read metrics, update resampler ratio

Beta Routine: Run pick_best_epsilon() per block

MIMO Calibration

- **Phase/Gain Estimation**
  Transmit known tone/preamble, estimate per-antenna offsets on PS
- **Compensation**
  Apply complex scalar before combining to align arrays

05

MIMO Extension

From SISO to 2×2 diversity and spatial multiplexing

MIMO EXTENSION · DIVERSITY

2×2 MIMO Diversity Combiner

Hardware Requirements

Dual TX Chains

Two DAC+amp+transducers with sample-synchronous operation and identical preambles. Optional shared reference clock for improved synchronization.

Dual RX Chains

Two ADC+preamp+hydrophones with synchronized sampling and per-channel gain/phase calibration capability.

PL Architecture (2×2 Diversity)

1. **Per-Antenna RX IP**
   Duplicate RX chain up to FFT output for each antenna: $Y_k^{(1)}$, $Y_k^{(2)}$
2. **Differential Detection per Antenna**
   Compute tentative symbols: $S_k^{(i)} = Y_k^{(i)} \times Y_{k-1}^{(i)*}$
3. **Diversity Combiner**
   SNR-weighted combining of symbol decisions

SNR-Weighted Combining

Weight Calculation

$$w_i = |Y_{k-1}^{(i)}| / (|Y_{k-1}^{(1)}| + |Y_{k-1}^{(2)}| + \varepsilon)$$

Where ε is a small floor to prevent division by zero

Combined Symbol

$$S_k = w_1 \times S_k^{(1)} + w_2 \times S_k^{(2)}$$

Combiner Modes

Mode 0	Mode 1	Mode 2
Equal Weight	SNR-Weighted	Select-Best

PS Calibration

Estimate relative phase and gain using preamble, apply complex scalar before combining to align arrays

Implementation: Combiner HDL module takes $Y_k^{(1)}$, $Y_k^{(2)}$ and previous magnitudes as input, outputs weighted sum S_k to slicer.

MIMO EXTENSION · ADVANCED ALGORITHMS

Beta Algorithm & Spatial Multiplexing

Beta Algorithm (Block-Level Residual Doppler)

Objective

Correct residual Doppler shift per block using pilot-aided hypothesis testing on PS

Algorithm Steps

1. For each block, test grid of candidate ε values
2. Rotate FFT bins: Y_k → Y_k · e^(-j2πkε)
3. Measure differential consistency on pilots
4. Select ε that maximizes pilot alignment metric

Candidate Grid

$$\varepsilon \in \{-2, -1.5, -1, -0.5, 0, 0.5, 1, 1.5, 2\} \times 10^{-3}$$

Cycles per subcarrier index (normalized frequency)

Implementation

PS computes best epsilon, writes to RX IP REG_EPSILON_SEL. PL applies rotation to all bins before detection.

Spatial Multiplexing Roadmap

TX Processing

Independent data streams per antenna on same subcarrier grid. Identical preambles for synchronization.

RX Processing Requirements

- ✓ Per-antenna FFT (already implemented for diversity)
- ✓ Pilot-aided linear equalization per subcarrier (ZF/MMSE)
- ✓ 2×2 channel matrix estimation H_k on sparse pilot grid
- ✓ Interpolation of H_k estimates across frequency

Differential + Equalization Approach

Apply ZF H_k^(-1) to recover streams, then differential detection per stream

$$\hat{S} = H_k^{-1} \cdot Y_k \rightarrow \text{Diff Detect} \rightarrow \text{Bits}$$

Prerequisites

Increased pilot density (every 8 bins), stable Beta correction enabled, robust Doppler control

Implementation Sequence

1. Validate 2×2 diversity combining
2. Enable Beta algorithm per block
3. Increase pilot density (every 8 bins)
4. Implement H_k estimation + ZF equalizer

06

Implementation Deliverables

Complete blueprint for deployment and validation

IMPLEMENTATION PACKAGE

Design Files & Common Pitfalls

Deliverables Checklist

Simulink Models
TX/RX with parameter blocks, test harness, channel model

HDL IP Cores
Mapper, differential encoder/decoder, IFFT/FFT, CP, correlator

Vivado Design
Block diagram, constraints, timing reports

PS Application
DMA, control/monitor, logging, BER/MSE computation

Test Reports
Loopback BER, resource usage, Fmax, power

Field Logs
Tank/pool BER/BLER/MSE vs scenarios, multipath profiles

MIMO Pilot
Dual-chain hardware, per-antenna FFT, combining

Common Pitfalls & Solutions

Doppler Underestimated
Symptom: BER spikes with small motion. **Solution:** Shrink block length or increase Δf (reduce K)

CP Too Short
Symptom: ISI from multipath exceeding T_g. **Solution:** Increase CP or use windowed overlap-and-add

AXI Stalls
Symptom: DMA underflow. **Solution:** Double-buffering, larger bursts, monitor TLAST

Word Length Issues
Symptom: Saturation/clipping in FFT/mixers. **Solution:** Add guard bits, profile dynamic range

Analog Saturation
Symptom: Non-linear distortion. **Solution:** Conservative gains, verify PA/preamp linearity

Key Performance Metrics

BER Bit Error Rate	**BLER** Block Error Rate
MSE Mean Square Error	**Fmax** Max Frequency

MATLAB Script

FIR coefficient generation for 50× interpolator/decimator:

```
h = fir1(512, fp/(fs/2), kaiser(513, 8.6));
h = h / sum(h);
save('fir_interp_decim_512.mat', 'h');
% Export to .coe for Vivado
```

IMPLEMENTATION BLUEPRINT

From Simulink to Deployment

A complete, step-by-step implementation blueprint for MIMO-OFDM underwater acoustic communication systems on Zynq FPGA platforms

125 kHz

Center Frequency

500 kHz

Sample Rate

2×2 MIMO

Diversity + Spatial

Complete implementation guide · Simulink to HDL · FPGA-ready IP cores · Testing & validation