A Low-Noise Chopper Amplifier Designed for Multi-Channel Neural Signal Acquisition

Deng Luo, *Student Member, IEEE*, Milin Zhang, *Senior Member, IEEE*, and Zhihua Wang, *Fellow, IEEE*

***Abstract*— This paper proposed the design of a low-noise, low total harmonic distortion (THD) chopper amplifier for neural signal acquisition. A dc servo loop (DSL) based on active Gm-C integrator is proposed to reject the electrode-dc-offset (EDO). Architecture of a complementary input very low-transconductance (VLT) operational transconductance amplifier (OTA) was proposed and integrated in the active Gm-C integrator to improve the linearity as well as to reduce the noise, featuring a transconductance ranging from 45 pS to a few nS. The proposed amplifier was fabricated in a TSMC 0.18-μm CMOS process, occupying an area of 0.2 mm^2, featuring a power consumption of 3.24 μW/channel under a 1.8-V supply voltage. The THD for a 5-mV$_{pp}$ input is lower than −61 dB. An input-referred thermal noise power spectral density (PSD) of 39 nV/$\sqrt{\text{Hz}}$ is measured. The measured input-referred noise is 0.65 μV$_{rms}$ in the 0.3–200-Hz frequency band and 2.14 μV$_{rms}$ in the 200-Hz–5-kHz frequency band, respectively, leading to a noise-efficiency factor of 2.37 (0.3–200 Hz) and 1.56 (0.2 k–5 kHz). In addition, the high-pass corner frequency can be precisely configured and linearly adjusted with the external bias current from 0.35 to 54.5 Hz.**

***Index Terms*— Active Gm-C integrator, chopper amplifier, complementary input operational transconductance amplifier (OTA), high linearity, low-noise amplifier, very low transconductance (VTL) OTA.**

I. Introduction

BRAIN–machine-interface (BMI) has been widely used in neuroprosthetics and neuromodulatory system, taking the advantages of the development in microelectrode, microelectronics, and computing technologies [1], [2]. Neural signal acquisition plays a critical role in a BMI system to close the loop [3]–[5]. The target signal varies while different electrodes are used or different detection locations are applied. Typically, local field potentials (LFPs) and action potentials (APs) are captured using an invasive penetrating electrode. The amplitude of LFP and AP is typically in the order of tens of microvolts to a few millivolts. The frequency of LFPs distributes from sub-Hz to about 200 Hz, and APs occupy a frequency band from 200 Hz to 5 kHz [6], [7].

In order to perform the LFPs and APs acquisition with high precision, an analog-front-end (AFE) features input-referred noise (IRN) as low as to μV level is required. In addition, the performance of low-power consumption is also expected to extend the battery life, as well as to reduce self-heating of the implanted device for safety [8]. However, there is a tradeoff between the noise and power, which is typically quantitatively measured in terms of noise-efficiency factor (NEF). The traditional capacitive-coupled instrumental amplifier (CCIA) features a low NEF, as well as a simple structure [9]. Different techniques, such as current splitting, source degeneration, complementary input, current reuse, and partial operational transconductance amplifier (OTA) sharing architecture [10]–[13] have been reported in the literature to reduce the NEF of a capacitive-coupled amplifier. In [10], an NEF of 3.09 is achieved by employing current scaling, current splitting, and bottom-transistor source degeneration to reduce the IRN. A complementary input-based OTA [14] can double the effective transconductance without increasing the bias current. Reference [12] proposed the current reuse technique enabling a reduction of NEF to 1.07 or even further by a stacking inverter. However, the capacitive-coupled amplifiers suffer from flicker noise, greatly reducing the performance of LFP signal acquisition. In order to obtain less than 1 μV$_{rms}$ IRN, the chopper-stabilized technique can be utilized, which pushes the $1/f$ frequency corner to sub-Hz [15].

One of the main challenges in chopper-stabilized amplifier design, as proposed in [15], is how to create a high-pass corner to filter out the electrode-dc-offset (EDO). Different from the capacitive-coupled amplifier, which features a high tolerance to the EDO rail-to-rail inherently, the chopper-stabilized amplifier cancels EDO by integrating an active feedback loop, denoted as dc servo loop (DSL). Reference [15] proposed a switched-capacitor integrator-based DSL design, realizing up to ±50-mV EDO cancellation, but requiring an 800-pF large on-chip capacitor with high silicon area consumption to achieve sub-Hz high-pass corner. A modified design is reported in [16] to reduce the silicon area, but sacrificing the IRN of the overall system by 6.7 uVrms (11.1×) in the band of 0.5–100 Hz, which is unacceptable for the application of LFP signal acquisition. The back-to-back pseudoresistor is widely used as an area-efficient method to create low high-pass corner while achieving low noise [17], [18]. However, the value of the pseudoresistor is extremely sensitive to process–voltage–temperature (PVT) variations, which can be

Manuscript received November 16, 2018; revised March 15, 2019; accepted April 12, 2019. Date of publication June 25, 2019; date of current version July 23, 2019. This paper was approved by Associate Editor Hoi-Jun Yoo. This work was supported in part by the Beijing Innovation Center for Future Chip, in part by the Beijing National Research Center for Information Science and Technology, in part by the National Natural Science Foundation of China under Grant 61674095, and in part by the Thousand Youth Talents Plan. *(Corresponding author: Milin Zhang.)*

D. Luo and Z. Wang are with the Institute of Microelectronics, Tsinghua University, Beijing 100084, China.

M. Zhang is with the Department of Electronic Engineering, Tsinghua University, Beijing 100084, China (e-mail: zhangmilin@tsinghua.edu.cn).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2019.2913101

varied by a factor of 100 [7]. In addition, the nonlinearity of the pseudoresistor causes poor performance with large output swing. For LFPs and APs acquisition applications, with an expectation of μV level IRN for the amplifier and approximately 10-bit ADC resolution [19], up to 60-dB dynamic range is required, which is almost impossible for the pseudoresistor-based structure, even with an elaborate bias scheme [20]. In [21], a digital low-pass filter is used for EDO cancellation. The quantization noise was successfully suppressed below the 1-μV thermal noise level, but a digital-to-analog converter (DAC) with higher than 17-bit resolution is required, which will greatly increase the complexity of the system. In addition, a total harmonic distortion (THD) of only -48 dB at 1-mV_{pp} input voltage is reported in [21].

To summarize, solutions to achieve a low-frequency high-pass corner have been reported in the literature, but a few can realize a good balance among noise, linearity, and accuracy. Pseudoresistor is low noise, but suffering from poor linearity and inaccuracy due to its high sensitivity to PVT variations. The switch-capacitor integrator features higher accuracy with high linearity but suffers from a poor noise performance due to noise aliasing [16].

This paper proposed an architecture of a chopper-stabilized amplifier designed for a multi-channel neural recording system, featuring a good balance between power, noise, and linearity, by employing an active Gm-C-based DSL. The proposed active Gm-C-based DSL achieves high linearity while maintaining low noise. The rest of this paper is organized as follows. Section II reviews the state of the art of very low transconductance (VLT) OTA designs, which is the key module in the chopper-stabilized amplifier. Section III introduces the proposed complementary input VLT OTA design. By using the proposed complementary VLT OTA, a low-noise chopper-stabilized neural signal amplifier was proposed in Section IV, including the detailed architecture design of each module and a noise analysis. Section V illustrates the experimental results, while Section VI concludes the entire work.

II. Design Requirements Analysis and Review of VLT OTA Designs

A. Design Requirements Analysis

Fig. 1(a) shows an overview of the proposed chopper stabilization-based neural signal amplifier design. It consists of a differential low-noise OTA and an active Gm-C integrator-based DSL. The proposed DSL features a very large time constant integrator based on the active Gm-C structure by implementing a VLT OTA, as shown in Fig. 1(b). The requirements of the VLT OTA are discussed as follows.

The transfer function of the proposed chopper amplifier is shown in Fig. 1(c). The high-pass corner frequency f_{hp} can be calculated as

$$f_{hp} = \frac{f_{\text{int},ugb} C_{hp}}{C_{fb}} \tag{1}$$

where $f_{\text{int},ugb}$ is the unity-gain bandwidth of the integrator, which is defined by $g_{m,\text{VLT}}/2\pi C_{\text{int}}$, and C_{hp} is approximately equal to twice the capacitance of C_{fb}.

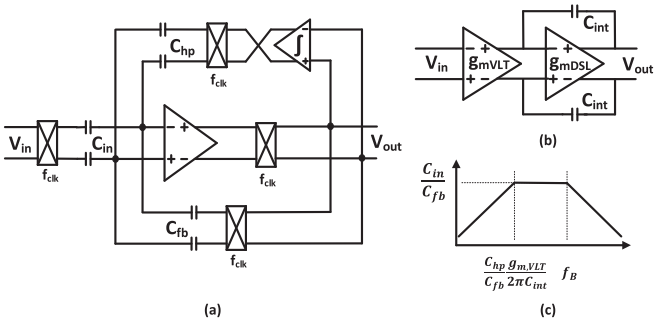


Fig. 1. (a) Schematic of the chopper-stabilized amplifier, consisting of a low-noise OTA and a DSL. (b) Active Gm-C integrator used in DSL. (c) Transfer function of the chopper amplifier using the active Gm-C integrator.

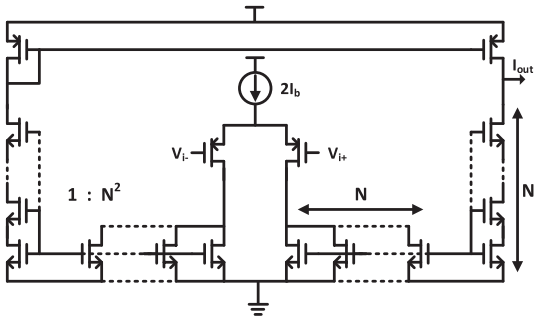


Fig. 2. Symmetrical OTA with series–parallel current division to reduce transconductance.

For LFP recoding, smaller than 0.5 Hz f_{hp} is required. According to (1), $f_{\text{int},ugb}$ of around 0.25 Hz is expected, which means that a very large time constant integrator is needed. The integrator capacitance C_{int} is set to 40 pF to achieve a good balance between the area consumption and noise. Thus, $g_{m,\text{VLT}}$ must be smaller than 63 pS, which places a great challenge for on-chip implement. Consider the scenario of invasive neural signal acquisition, the input linear range of the chopper-stabilized amplifier should be at least 4 mV_{pp}, and the closed-loop gain of the amplifier is set to 40 dB, which means that a linear input range of 400 mV_{pp} is required for the VLT OTA design.

B. Review of VLT OTA Designs

Various VLT OTA topologies have been reported in the literature. An extremely low bias current is applied in [22], leading to an extremely low transconductance. However, the input linear range is limited to 100 mV_{pp}, as the input transistors operate in the subthreshold region. Current cancellation technique is utilized to divide the OTA transconductance by a desired factor [23]. However, it is very sensitive to the mismatch and noise, leading to a limited reduction factor of about 20. Current division is an alternative method to realize low transconductance, which simply uses current mirrors with large division factors [24]. However, it is area hungry. The active area of the VLT OTA is roughly 0.25 mm^2. The area efficiency can be improved by using a series–parallel current division in OTA, as shown in Fig. 2. An OTA features a transconductance of 89 pS with a linear range of $\pm$500 mV

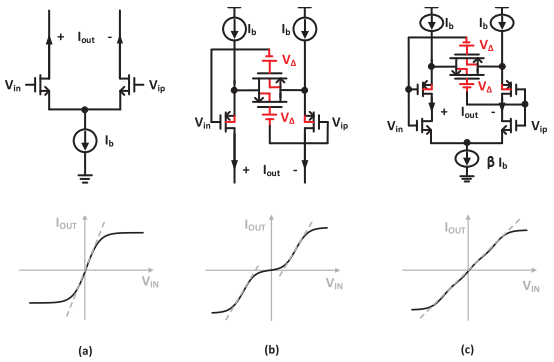


Fig. 3. (a) Classical differential nMOS pair OTA input stage. (b) Differential pMOS pair OTA input stage with source degeneration transistors. (c) Proposed complementary OTA input stage.

are reported in [25] by employing the series–parallel current division scheme with a division factor of 784 and consuming an area of 0.15 mm^2. Although the area efficiency is obviously improved, there is still room for further improvement to better fit the requirement rising from multi-channels neural acquisition applications. In this paper, a low-noise, low-power consumption amplifier is proposed. A complementary input, weak inversion region biased VLT OTA with extremely low bias current is applied in the proposed design. A much lower division factor is achieved with the same transconductance while compared with the design reported in the literature (see [25]). The noise is greatly reduced since higher g_m/I_d is applied. In addition, the silicon area efficiency and power consumption are also improved in the proposed design.

III. Design of a VLT OTA With Complementary Input Stage

A. Design of a Complementary Input Stage for OTA

The differential nMOS pair is widely used in the classical OTA design as the input stage, as shown in Fig. 3(a). A very low tail current is used to achieve VTL. The nMOS pair is biased in a weak inversion region. The input linear range is limited to 100 mV_{pp}. Fig. 3(b) shows a differential pMOS pair OTA input stage with a source degeneration technique. Different from the traditional source degeneration technique, V_Δ, as shown in Fig. 3(b), is employed as the input bias offset of the source degeneration transistors to provide an extra degree of freedom. The input pair and the source degeneration transistors, featuring the same size, are biased in the deep subthreshold region. When the input voltage is lower than V_Δ, the current passing through the source degeneration transistors is very small due to the bias offset voltage V_Δ. The source degeneration transistors act as an extremely large resistor. Considering the source negative feedback effect, the effective transconductance of the input differential pair is nearly zero. When the input voltage increases to be closed to V_Δ, the effective impedance of the source degeneration transistors decreases dramatically, which means that the source degeneration transistors work normally to extend the linear range around an input voltage of V_Δ. When the input voltage further increases, one of the input transistors will be turned off. Comparing Fig. 3(a) and (b), the linear input point of the classical differential nMOS pair is around zero, while the linear input point of the pMOS pair with source degeneration transistors is shifted to $\pm V_\Delta$.

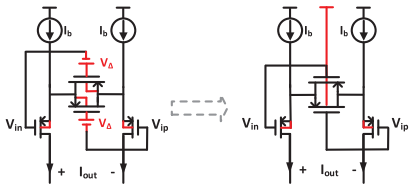


Fig. 4. Body effect is used in the proposed design to generate equivalent bias offset voltage of the source degeneration transistors.

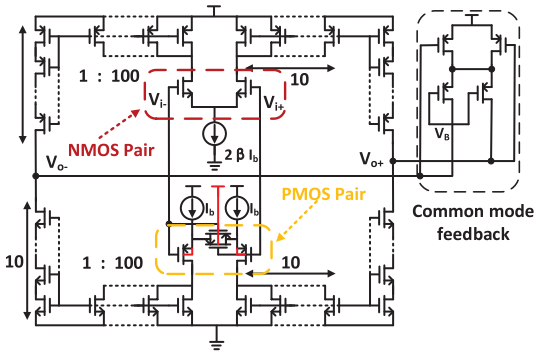


Fig. 5. Schematic of the proposed VLT OTA with a complementary input stage.

This paper proposed a complementary input stage design technology for OTA, as shown in Fig. 3(c). It combines the nMOS pair with the pMOS pair with a proper ratio to extend the input linear range. An equivalent offset voltage of the source degeneration transistors is generated by applying a threshold of the source degeneration transistors larger than that of the input differential pair, as shown in Fig. 4. If a larger threshold is applied, a larger input voltage is required to turn on the device with the same function of the offset voltage. The bulks of the differential pair are connected to the source, while the bulks of source degeneration transistors are connected to the power line. The threshold voltage is given by

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\phi_F|} - \sqrt{|2\phi_F + V_{SB}|}\right) \tag{2}$$

where V_{TH0} is the threshold voltage with $V_{SB} = 0$, γ is the body-effect constant, ϕ_F is the Fermi potential of the substrate, and V_{SB} is the voltage between the source and the bulk. The equivalent offset voltage V_Δ can be given by

$$V_\Delta = \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right). \tag{3}$$

In the proposed design, a simulated V_Δ value of 0.149 V is achieved by biasing the source degeneration transistors with V_{DD}.

B. Architecture of a Complementary Input VLT OTA

Based on the proposed complementary input stage, the architecture of a complementary input VLT OTA is proposed, as shown in Fig. 5. The series–parallel current division

scheme is used in the proposed design. It also employed the proposed linearizing method to extend the input linear range while reducing the noise and area consumption. The output current of the VLT OTA is contributed by the nMOS pair and the pMOS pair together. The ratio between the bias current of the nMOS input pair and that of the pMOS input pair is denoted as β. The series–parallel current division scheme is applied to the nMOS pair and the pMOS pair separately. There are ten transistors connected in parallel and ten transistors connected in series to divide the input current by a ratio of 100. Thus, a VTL can be achieved.

Assuming that the two input transistors match perfectly and ignoring the channel length modulation effects, the output differential current of pMOS pair can be calculated as

$$I_d \approx 2I_b \frac{e^{\frac{-\kappa V_\Delta}{V_T}}\left(e^{\frac{\kappa V_d}{V_T}} - e^{\frac{-\kappa V_d}{V_T}}\right)}{\zeta + e^{\frac{-\kappa V_\Delta}{V_T}}\left(2 + e^{\frac{\kappa V_d}{V_T}} + e^{\frac{-\kappa V_d}{V_T}}\right)} \tag{4}$$

where V_d is the input differential voltage, I_b is the bias current for each transistor in the differential pair, V_Δ is defined by (3), V_T is the thermal voltage of 26 mV at room temperature, ζ is the ratio between the W/L of the pMOS pair and the source degeneration transistors, and κ is the subthreshold slope factor that depends on the progress. The output current of the nMOS pair can be expressed as

$$I_d = 2\beta I_b \frac{e^{\frac{\kappa V_d}{V_T}} - 1}{e^{\frac{\kappa V_d}{V_T}} + 1}. \tag{5}$$

Based on (4) and (5), the output differential current of the proposed OTA is expressed as

$$I_d = \frac{2I_b}{N}\left(\beta \frac{e^{\frac{\kappa V_d}{V_T}} - 1}{e^{\frac{\kappa V_d}{V_T}} + 1} + \frac{e^{\frac{-\kappa V_\Delta}{V_T}}\left(e^{\frac{\kappa V_d}{V_T}} - e^{\frac{-\kappa V_d}{V_T}}\right)}{\zeta + e^{\frac{-\kappa V_\Delta}{V_T}}\left(2 + e^{\frac{\kappa V_d}{V_T}} + e^{\frac{-\kappa V_d}{V_T}}\right)}\right) \tag{6}$$

where N is the current division factor, which is set to 100. I_b is the bias current for each transistor of the pMOS input pair, which is set to 0.5 nA. In (6), β, ζ, and V_Δ are the three independent variables. The goal of the proposed design is to achieve a high linearity with a larger linear input range. The nonlinearity of I_d can be qualified as

$$e = \frac{\sqrt{\int_{-I_{d,\max}}^{I_{d,\max}} {I_{d\Delta}}^2 \, dI_d}}{\sqrt{\int_{-I_{d,\max}}^{I_{d,\max}} {I_d}^2 \, dI_d}} \tag{7}$$

where $I_{d\Delta}$ is the deviation of I_d to an ideal one, which is also called residual, while $I_{d,\max}$ represents the linear input range. There is a tradeoff between the nonlinearity and the linear input range, which is shown in Fig. 6(a). It is calculated according to (6) by sweeping β, ζ, and V_Δ. In this paper, the maximum target signal is 2.5 mVp. With a gain of 40 dB, the input of the VLT OTA can be 250 mVp. However, according to the simulation, THD is smaller than -60 dB, when $I_{d,\max}$ is set to 250 mVp. To meet the requirement of THD, $I_{d,\max}$ is set to 200 mVp. A voltage divider is employed to enhance the linear range from 200 mVp to 250 mVp, as addressed in Section IV-C.

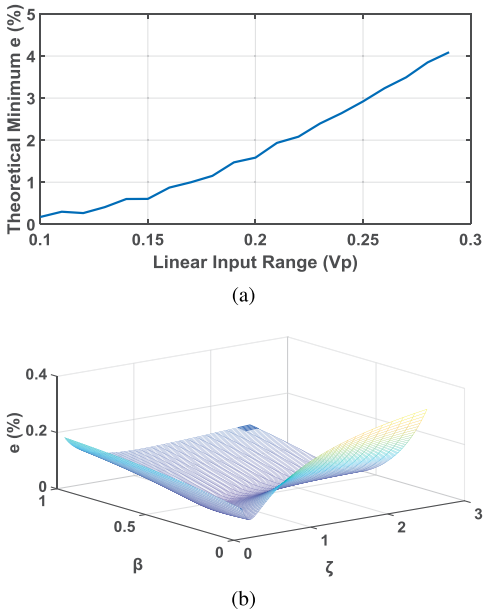


Fig. 6. Plot of (a) linear input voltage versus the achievable minimum nonlinearity e. (b) e versus β and ζ.

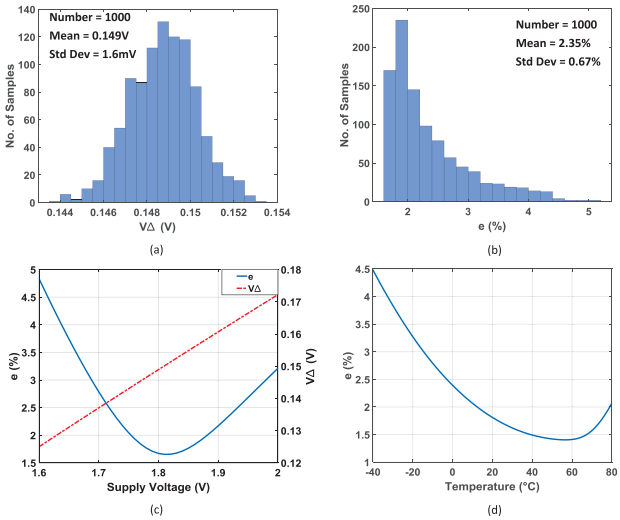


Fig. 7. Simulation results of (a) V_Δ versus process variations, (b) e versus process variations, (c) e versus supply voltage, and (d) e versus temperature.

The value of e can be optimized by tuning β and ζ with a fixed $I_{d,\max}$ value. As mentioned earlier, V_Δ is set to 0.149 by biasing source degeneration transistors with supply voltage.

Fig. 6(b) shows the relationship between e and β and ζ. A minimum e value of 1.6% is achieved with a β value of 0.46 and a ζ value of 0.82, respectively.

PVT sensitivity is important to the performance of the proposed design. V_Δ varies with the process variations, as shown in Fig. 7(a). With 1000 runs of Monte Carlo simulation, V_Δ features a standard deviation of 1.6 mV. Fig. 7(b) shows the nonlinearity factor e with process variations. An average e value of 2.35% is achieved. According to (3), V_Δ is sensitive to the supply voltage. Fig. 7(c) shows the simulated relationship between V_Δ or e and supply voltage, respectively. In order to achieve less than 2% of e, the supply voltage should be in the

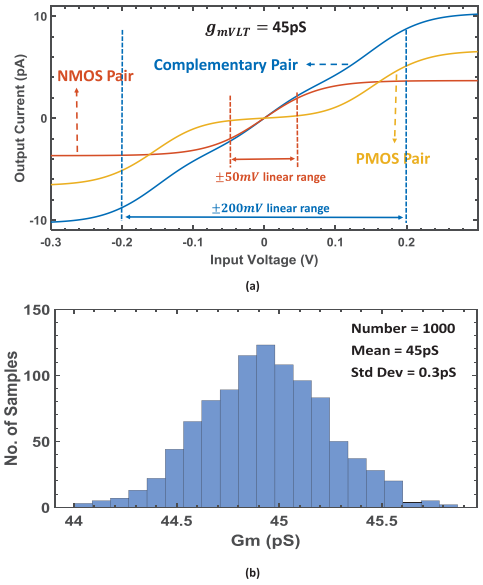


Fig. 8. (a) Simulation results of the output current of the VLT OTA versus the input voltage. Compared with the OTA with a single nMOS pair as the input stage, the proposed one with a complementary input stage increases the linear range by four times, from ±50 to ±200 mV. (b) Monte Carlo simulation with 1000 runs. The simulation results show a high robustness of the proposed VLT OTA against the process variation.

range of 1.75–1.88 V. A power supply insensitive bias circuit can be designed to enlarge the supply voltage range. Fig. 7(d) shows the simulated relationship between e and temperature. It clearly shows that the proposed design is not very sensitive to the changes in temperature under the room temperature.

The simulated output current of the proposed VLT OTA versus the differential input voltage is plotted, as shown in Fig. 8(a). When β is set to 0.5, the linear range is enhanced by four times, from ±50 to ±200 mV by using the proposed complementary input stage. The implementation of the common-mode (CM) feedback loop is shown in Fig. 5 as well. The current flowing through the nMOS in the output branch is larger than that of the pMOS since the bias current of the pMOS pair is larger than that of the nMOS pair. The CM feedback loop integrates a pair of pMOS branch to compensate for the current gap between the output nMOS and pMOS. Two pMOS transistors worked in the triode region are used to sense the output of the VLT OTA to adjust the current of the compensating pMOS branch. Thus, the CM output of the VLT OTA can be set to a proper value. In this design, the CM output is set to 1.4 V. Note that the output of the proposed VLT OTA is connected to a virtual ground node, which is the input of an OTA. Thus, the CM feedback loop performs little influence on the linearity.

The proposed VLT OTA features high robustness against the process. A Monte Carlo simulation with 1000 runs is performed, as shown in Fig. 8(b). The simulated g_{mVLT} value is 45 pS with a standard deviation of only 0.3 pS. The active area of the proposed VLT OTA is only 0.0055 mm^2. Compared with the state-of-the-art series–parallel current-based OTA design [25], the area consumption is reduced by a factor of 27.3.

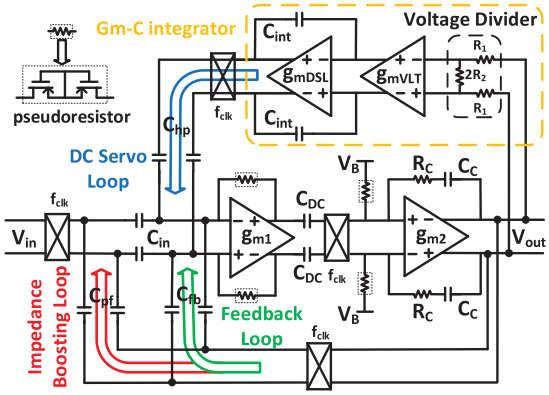


Fig. 9. Schematic of the proposed two-stage chopper-stabilized amplifier.

Compared with thermal noise, the flicker noise of the VLT OTA can be ignored. The corner frequency of the flicker noise is lower than 0.1 mHz according to the simulation. By applying the thermal model in the deep subthreshold region, the output current noise in Fig. 5 can be calculated as

$$\overline{i_{n,\mathrm{out}}^2} = \frac{8kT}{V_T} I_b \left(\frac{1}{N} + \frac{2}{N^2}\right). \tag{8}$$

According to (6), when the input voltage is zero, the transconductance of the proposed VLT OTA in Fig. 5 can be given by

$$g_m = \frac{\beta\kappa I_b}{N V_T}. \tag{9}$$

According to (8) and (9), the IRN in Fig. 5 can be expressed as

$$\overline{v_{n,in}^2} = \frac{\overline{i_{n,\mathrm{out}}^2}}{g_m^2} \approx \frac{8kT}{\beta\kappa g_m}. \tag{10}$$

IV. Design of the Proposed Low-Noise Chopper-Stabilized Amplifier

A. System Overview of the Proposed Chopper Amplifier

The proposed chopper-stabilized neural recording amplifier is shown in Fig. 9. It consists of: 1) a two-stage Miller-compensated OTA; labeled as g_{m1} and g_{m2}; 2) an input impedance boosting loop; 3) an active Gm-C integrator-based DSL using the proposed VLT OTA, labeled as g_{mVLT}; and 4) a capacitive feedback loop.

The two-stage Miller-compensated OTA dominates the linearity performance in the high-frequency band, while in the low-frequency band, the linearity performance is decided by the active Gm-C integrator. As mentioned earlier, a complementary input scheme was employed in the proposed Gm-C integrator to enhance the linear range. In addition, the resistance divider is utilized as a pre-stage to further improve the linearity performance.

In the proposed design, C_{in} is set to 5 pF, while f_{clk} is set to 20 kHz. The equivalent input impedance is calculated as 5 MΩ. A positive feedback loop as addressed in [16], which can provide required current to the input switched-capacitor resistor, is also integrated into the proposed work.

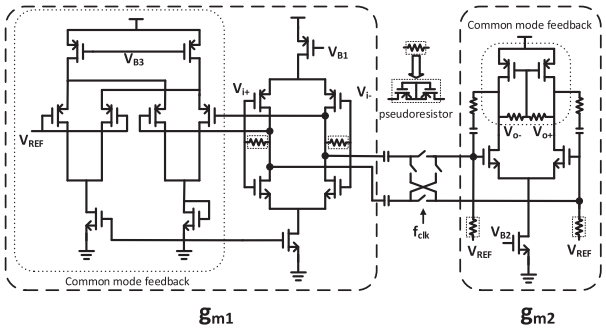


Fig. 10. Detailed schematic of the two-stage low-noise OTA in the chopper-stabilized amplifier, which is labeled as g_{m1} and g_{m2} in Fig. 9.

The capacitance of C_{pf} is set to 53 fF according to the post-layout simulation to eliminate the parasitic capacitor effect. Thus, the differential input impedance is boosted to 440 MΩ at 50 Hz.

B. Design of the Low-Noise Two-Stage OTA

Fig. 10 shows the architecture of the low-noise two-stage Miller-compensated OTA. A pair of capacitors $C_{\rm dc}$, as shown in Fig. 9, is used to block the dc-offset, which may propagate to the output ripple. A large resistor connected the input and output of the first stage is used as a dc-feedback loop, as well as to establish a stable dc bias for the input pairs [26]. To secure the stability, the Miller-compensated capacitor with an adjusting zero resistor is employed.

In the second stage, a back-to-back pseudoresistor is used to bias the input pairs. It is important to note that the input swing of the second stage is small enough to achieve high linearity. Since the noise of the second stage is much smaller than the first stage, the second stage can be biased to a relatively low current for better power efficiency. However, the resistive sensing scheme is employed for the CM feedback to improve the linearity. The bias current of the second stage must be high enough to meet the driving capability requirement. A tradeoff is performed to balance the power-efficiency requirement and the linearity requirement, and the bias current is set to 400 nA.

A complementary input-based OTA is used to double the effective transconductance without increasing the bias current. The theoretical NEF limit can be reduced by a factor of $\sqrt{2}$. Since the flicker noise of the two-stage OTA is removed from the baseband due to the chopper structure, leaving only the thermal noise. For low-noise design, the input transistors are biased in the deep subthreshold region. The transconductance of a subthreshold MOSFET can be expressed as

$$g_m \approx \frac{\kappa I_D}{V_T} \tag{11}$$

where I_D is the drain current of the input transistor. The current-noise power spectral density (PSD) of the subthreshold MOSFET can be modeled as

$$\overline{i_{ni}^2} = 4kT\frac{1}{2\kappa}g_m. \tag{12}$$

When ignoring the noise contributed from the second stage, the IRN PSD of the two-stage OTA can be expressed as

$$\overline{v_{ni}^2} = 4\frac{\overline{i_{ni}^2}}{(2g_m)^2} = 2kT\frac{V_T}{\kappa^2 I_D}. \tag{13}$$

According to (13), the complementary input structure can reduce the IRN by a factor of $\sqrt{2}$ while compared with one without such a structure [10]. In this proposed design, the bias current of the input pairs are set to 1 μA ($2I_D = 1$ μA). A theoretical IRN of 30 nV/$\sqrt{\rm Hz}$ is expected.

C. Design of the DC Servo Loop

The DSL integrates a very large time constant integrator based on the active Gm-C structure, which is implemented by the proposed VLT OTA as discussed earlier. The EDO cancellation range is directly determined by C_{hp} as

$$V_{\rm EDO} = \frac{V_{DD}C_{hp}}{C_{\rm in}}. \tag{14}$$

The input capacitance $C_{\rm in}$ is set to 5 pF with a supply voltage of 1.8 V. In order to achieve a maximum $V_{\rm EDO}$ value up to 50 mV, according to (14), C_{hp} should be at least 139 fF. A voltage divider shown in Fig. 11(a) is used as the input stage of the integrator to improve the linearity. The high-pass frequency can then be calculated as

$$f_{hp} = \frac{\alpha C_{hp} g_{\rm mVLT}}{2\pi C_{fb} C_{\rm int}} \tag{15}$$

where α is the voltage division factor. In this proposed design, the voltage division factor of α is set to 0.8, while $g_{\rm mVLT}$ is 45 pS. A high-pass frequency corner of 0.4 Hz can be achieved. With the voltage divider, the linear range can be further enhanced from ±200 to ±250 mV. There is a tradeoff between the linearity and the noise. In order to enable a higher linear range, the noise will increase by a factor of $1/\alpha$.

The output of the DSL generates large spikes caused by the charge and discharge of the capacitor C_{hp} when the EDO generated at the electrodes is quite large. These spikes cause two problems: 1) the spikes pass from the output of the DSL to the output of the LNA. The spikes with an amplitude of 500 $\rm mV_{pp}$ can be observed at the output of the LNA according to simulation with an EDO of 50 mV and 2) the spikes at the DSL output can be kicked back to the input of $g_{m\rm DSL}$ through the integral capacitor $C_{\rm int}$ due to which $g_{m\rm DSL}$ may be unstable or even out of work. To solve this problem, a bypass capacitor C_{bp} of 10 pF is connected to the DSL output to provide the current when charging and discharging C_{hp}. The bypass capacitor ensures that $g_{m\rm DSL}$ works properly and reduces the spikes at the output of LNA to about 20 $\rm mV_{pp}$.

The bias current of $g_{\rm mVLT}$ can be switched between two modes. In the integrator mode, the bias current is 0.5 nA. At this situation, the high-pass frequency corner is 0.4 Hz. It will take a long time for the LNA to resume. To shorten the setting time, the bias current is switched to 100 nA to push the DSL working in the setting mode when the LNA is turned on.

Fig. 11(b) shows the schematic of the OTA used in DSL. A class-AB structure is used to enhance the driveability.

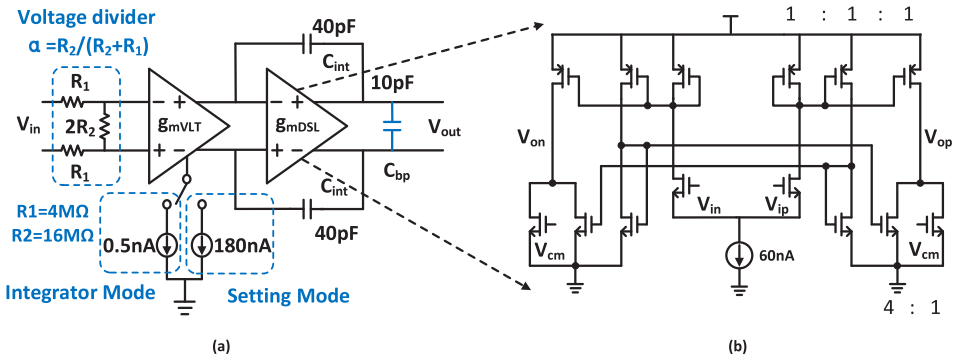


Fig. 11. (a) Architecture of the dc servo loop based on the Gm-C structure. A voltage divider is used as the input stage of the integrator to improve the linearity. (b) Schematic of the OTA $g_{m\mathrm{DSL}}$ used in DSL. A class-AB structure is used.

The total current of $g_{m\mathrm{DSL}}$ is only 200 nA, including the CM feedback loop.

The setting mode may cause instability of the design. The loop transfer function can be expressed as

$$Ls = \frac{2\pi AC_{fb}f_{hp}\left(1+\frac{s}{2\pi f_{hp}}\right)}{sC_{\mathrm{in}}\left(1+\frac{s}{2\pi f_{p1}}\right)\left(1+\frac{s}{2\pi f_{p2}}\right)} \tag{16}$$

where A is the dc gain of the two-stage OTA, as shown in Fig. 10. f_{p1} and f_{p2} are the poles of the two-stage OTA. A Miller compensation scheme is employed to realize an f_{p2} value much higher than f_{p1}, so as to reduce the correlation between f_{p2} and the circuit stability. A pole and a zero are introduced by the DSL. In order to achieve a phase margin of 60°, a relationship of

$$f_{hp} < 2f_{p1} \tag{17}$$

is expected. The simulated f_{p1} value is 170 Hz. A maximum f_{hp} of 340 Hz is expected according to (17). The simulated f_{hp} value in the integrator mode and the setting mode is 0.4 and 180 Hz, respectively. Thus, a phase margin of nearly 90° can be achieved in both the modes.

D. Noise Analysis

A noise equivalent model is built to analyze the noise performance, as shown in Fig. 12. The IRN PSD of the chopper-stabilized amplifier is calculated using the output noise PSD divided by the mid-band gain as follows:

$$\begin{aligned}\overline{v_{n,\mathrm{in}}^2} = {} & \overline{v_{ni,\mathrm{core}}^2}\left(\frac{C_{\mathrm{in}}+C_{fb}+C_{hp}}{C_{\mathrm{in}}}\frac{1}{1+\frac{2\pi f_{hp}}{S}}\right)^2 \\ & + \overline{v_{ni,g_{m\mathrm{DSL}}}^2}\left(\frac{C_{hp}}{C_{\mathrm{in}}}\frac{1}{1+\frac{2\pi f_{hp}}{S}}\right)^2 \\ & + \overline{v_{ni,g_{m\mathrm{VLT}}}^2}\left(\frac{1}{\alpha}\frac{C_{fb}}{C_{\mathrm{in}}}\frac{1}{1+\frac{S}{2\pi f_{hp}}}\right)^2\end{aligned} \tag{18}$$

where

$$f_{hp} = \frac{\alpha g_m C_{hp}}{2\pi C_{\mathrm{int}}C_{fb}} \tag{19}$$

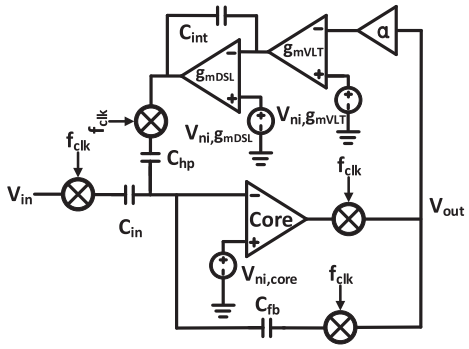


Fig. 12. Schematic of the proposed amplifier for noise calculation.

is the high-pass corner of the amplifier. According to (18), the ratio of the noise contribution to the IRN PSD between the core OTA and $g_{m\mathrm{DSL}}$ is equal to $(C_{\mathrm{in}}+C_{fb}+C_{hp})/C_{hp}^2$. Thus, the noise origins from $g_{m\mathrm{DSL}}$ can be omitted when compared with the noise from the core OTA.

Substituting (13) and (10) into (18), the total input-referred integrated noise from high-pass cutoff frequency f_{hp} to the low-pass filter cutoff frequency f_{lp}, which is typically 200 Hz for the LFP signal recording and 5 kHz for the AP signal recording, can be calculated as follows:

$$\begin{aligned}V_{ni,\mathrm{rms}} & = \sqrt{\int_{f_{hp}}^{f_{lp}} \overline{v_{n,\mathrm{in}}^2}\,df} \\ & = \sqrt{2kT\frac{V_T}{\kappa^2 I_D}\left(\frac{C_{\mathrm{in}}+C_{fb}+C_{hp}}{C_{\mathrm{in}}}\right)^2 f_{lp} + \frac{kTV_{\mathrm{EDO}}}{A\alpha\beta\kappa V_{DD}C_{\mathrm{int}}}}\end{aligned} \tag{20}$$

where A is the closed-loop gain of the chopper-stabilized amplifier, defined as $A = C_{\mathrm{in}}/C_{fp}$. According to (20), the total input-referred integrated noise consists of two parts: 1) the thermal noise from the core OTA and 2) the noise associated with the EDO cancellation range, the supply voltage, the closed-loop gain, the integration capacitance, and the voltage division factor. It resources from the VLT OTA. As mentioned earlier, a smaller voltage division factor α always leads to better linearity. However, according to (20),

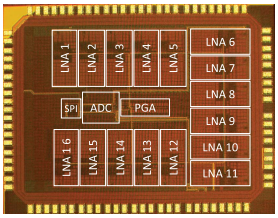


Fig. 13. Microphotography of the proposed chip, which has been fabricated in a TSMC 180-nm CMOS process, occupying a silicon area of 2.6 mm × 2 mm.

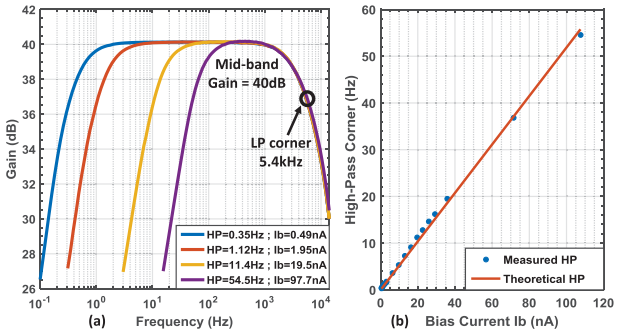


Fig. 14. (a) Measured frequency response of the fabricated chopper amplifier with adjustable high-pass corner frequency. (b) High-pass corner frequency versus the bias current.

a small voltage division factor may significantly increase the noise. A tradeoff between the noise performance and the linearity must be performed. For this application, V_{EDO} and V_{DD} are set to 50 mV and 1.8 V, respectively. Thus, the closed-loop gain A is set to 40 dB. The integration capacitor C_{int} is set to 40 pF as a tradeoff between the area consumption and the noise. The IRN resourced from the VLT OTA can be calculated as 0.31 uVrms.

V. Experimental Results

The proposed work has been fabricated in the TSMC 180-nm CMOS process, occupying a silicon area of 2.6 mm × 2 mm. Fig. 13 shows the microphotography of the proposed chip. The 16 integrated chips proposed low-noise chopper amplifiers for the neural signal acquisition of 16 independent channels. A programmable gain amplifier (PGA), an SAR ADC, and an serial peripheral interface (SPI) encoder are integrated as well for further signal amplifying, digitizing, and readout.

During the bench test, the chopping clock frequency is set to 20 kHz. The measured mid-band gain is 40 dB with a high-pass cutoff frequency of 0.35 Hz and a low-pass cutoff frequency of 5.4 kHz, as shown in Fig. 14.

The high-pass corner frequency can be precisely set and linearly adjusted by tuning the bias current of the Gm-C integrator-based DSL. Fig. 15(a) compares the theoretical noise density derived from Section III with the measured results. It clearly shows that the theoretical analysis and the measured results perfectly match. According to Fig. 15(a), the DSL dominates the noise density in the low-frequency band, and a noise corner frequency of 5.5 Hz is achieved. The input-referred thermal noise is 39 nV/$\sqrt{\text{Hz}}$. The measured

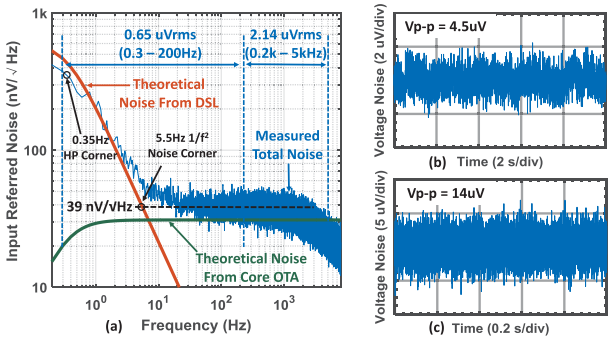


Fig. 15. (a) Comparison between the measured IRN (blue line) and the theoretically derived noises calculated by (13) (green line) and (20) (red line). (b) Input-referred peak-to-peak voltage noise in the frequency band of 0.3–200 Hz. 4.5 μV is achieved. (c) Input-referred peak-to-peak voltage noise in the frequency band of 200 Hz–5 kHz. 14 μV is achieved.

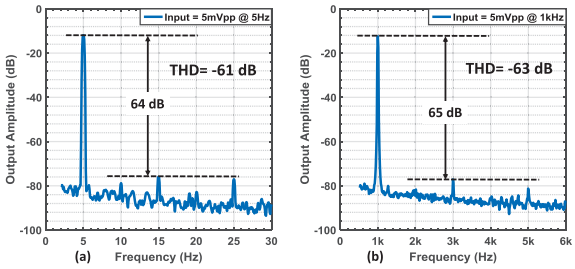


Fig. 16. (a) Measured harmonic distortion of the amplifier for a 5-mV$_{pp}$ input at 5 Hz. (b) Measured harmonic distortion of the amplifier for a 5-mV$_{pp}$ input at 1 kHz.

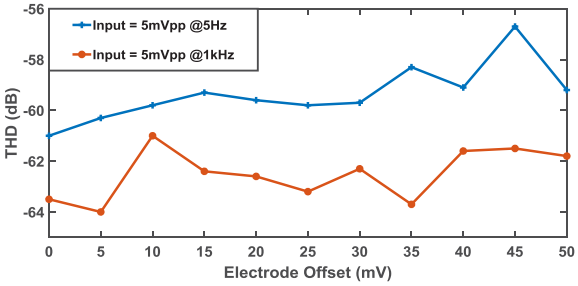


Fig. 17. Measured THD versus electrode offset for a 5-mV$_{pp}$ input at 5 Hz and 1 kHz separately.

integrated noise is 0.65 and 2.14 μV$_{rms}$ in the frequency band of 0.3–200 Hz and 0.2 k–5 kHz, respectively. An input-referred peak-to-peak voltage noise of 4.5 μV (0.3–200 Hz) and 14 μV (0.2 k–5 kHz) are measured, as shown in Fig. 15(b) and (c), respectively.

Fig. 16 presents the harmonic distortion for a 5-mV$_{pp}$ input at different frequencies. In the frequency band of 200–5 kHz, the THD is dominated by the core two-stage OTA, while DSL dominates in the frequency band from near dc to 200 Hz. According to the experimental results, a THD of lower than −61 dB is achieved. Fig. 17 shows the measured THD versus electrode offset with a 5-mV$_{pp}$ input at 5 Hz and 1 kHz, respectively. THD decreases slightly while the electrode offset is increased, especially at the low-frequency band. Neural signal acquisition suffers from CM interference (CMI). Thanks to the chopping scheme, a high common-mode rejection ratio

TABLE I

PERFORMANCE AND COMPARISON OF THE PROPOSED NEURAL AMPLIFIERS

Reference	[15] JSSC'07	[21] JSSC'15	[18] JSSC'15	[7] JSSC'17	[27] JSSC'17	[28] JSSC'18	[17] JSSC'18	[12] JSSC'18	**This work**
Topology	Chop.Amp	Chop.Amp	Chop.Amp	Chop.Amp	ΔΣ-based	ΔΣ-based	Chop.Amp	CCIA	**Chop.Amp**
Current/ch	1.11μA	4.6μA	0.9μA	2.33μA	0.525μA	1μA	4.5μA	0.25μA	**1.8μA**
Voltage	1.8V	0.5V	1.8V	1.2V	1.2V	0.8V	1.2V	1V	**1.8V**
IRnoise (V_{rms})	0.98μ (0.05-100Hz)	1.3μ (1-500Hz)	0.9μ (0.5-100Hz)	1.8μ (1-200Hz) 5.3μ (0.2k-5kHz)	1.13μ (0.1-500Hz)	0.99μ (1-500Hz)	0.44μ (0.5-100Hz)	5.5μ (10-10kHz)	**0.65μ (0.3-200Hz) 2.14μ (0.2k-5kHz)**
NEF	4.6 (0.05-100Hz)	4.76 (1-500Hz)	3.29 (0.5-100Hz)	7.4 (1-200Hz) 4.4 (0.2k-5kHz)	2.86 (0.1-500Hz)	1.81 (1-500Hz)	3.59 (0.5-100Hz)	1.07 (10-10kHz)	**2.37 (0.3-200Hz) 1.56 (0.2k-5kHz)**
Input Impedance	5MΩ	25MΩ	>500MΩ	1.6GΩ	1MΩ	26MΩ	1GΩ	—	**440MΩ**
THD	−60dB (10mVpp)	−48dB (1mVpp)	—	-76dB (40mVpp)	—	-71dB (31mVpp)	—	—	**−61dB (5mVpp)**
CMRR	>80dB	88dB	97dB	>78dB	90dB	81dB	>110dB	84dB	**>100dB**
Max.EDO	50mV	50mV	240mV	—	Rail-to-Rail	260mV	350mV	∞	**50mV**
Area/ch	1.7mm^2	0.025mm^2	—	0.071mm^2	0.013mm^2	0.024mm^2	—	0.097mm^2	**0.2mm^2**
Technology	0.8μm	65nm	0.18μm	40nm	0.13μm	65nm	65nm	0.18μm	**0.18μm**

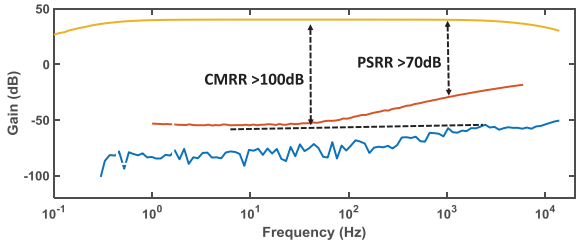


Fig. 18. Measured CMRR and PSRR.

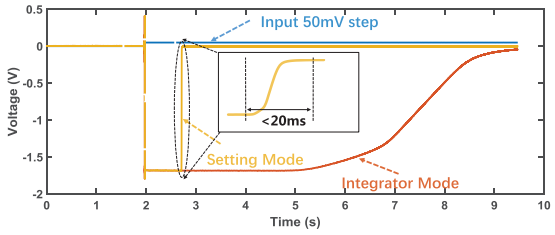


Fig. 19. Time-domain response of a 50-mV step input in the integrator mode and the setting mode, respectively.

(CMRR) can be achieved. The measured CMRR and power supply rejection ratio (PSRR) are shown in Fig. 18. A CMRR of 100 dB is achieved under a CMI of 200 mV$_{pp}$.

To test the response time in the integrator mode and the setting mode, a step input of 50 mV is performed, as shown in Fig. 19. The response time in the integrator mode can be larger than 10 s. While in the setting mode, less than 20 ms is needed for a full setting, once the setting switch is trigged. Fig. 20 shows the measured in vivo LFP without filtering recording from freely moving mice.

Table I compares the proposed work with state-of-the-art designs in the literature. Three different topologies of AFEs were compared. The traditional CCIA structure features high input impedance and rail-to-rail EDO but suffers from high flicker noise. The ΔΣ-based AFE designs feature high area efficiency, high tolerance of large EDO, and low noise.

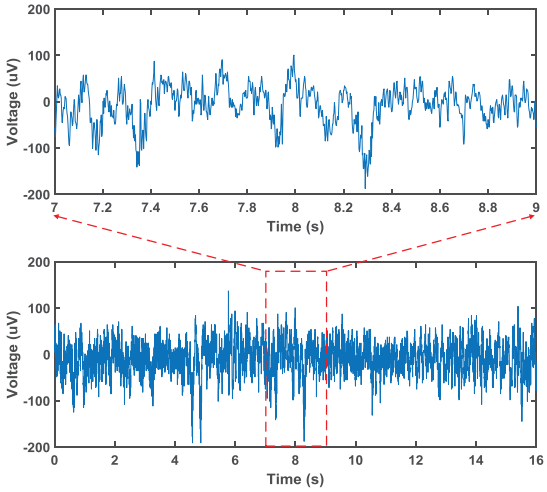


Fig. 20. Raw data of the in vivo LFP recording.

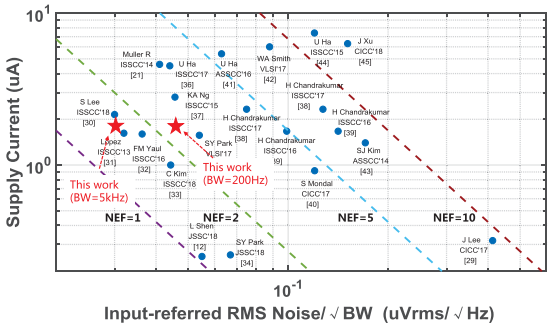


Fig. 21. Comparison with state-of-the-art AFE designs (see [12], [21], [29]–[45]) of the input-referred rms noise versus the supply current of the amplifier.

However, the input impedance is relatively small, and the bandwidth is limited. The chopper amplifiers are widely used with low flicker noise and high CMRR. However, the traditional DSL structures used in chopper amplifiers introduce

noise and cause nonlinearity. A novel VLT OTA-based DSL is proposed in this paper, achieving high linearity and low noise. Fig. 21 shows the input-referred rms noise versus the supply current of the amplifier. The proposed work features a low IRN while achieving a competitive NEF.

VI. Conclusion

In this paper, a low-noise, low-power, and low THD amplifier with chopper modulation topology is proposed for neural signal acquisition. Different from the traditional DSL designed based on the switched-capacitor technique or pseudoresistor, which suffers from either the high noise or the poor linearity, an active Gm-C integrator with a complementary input scheme is proposed to achieve high linearity while maintaining a low-noise performance. The proposed complementary input stage features a better linearity when compared with the traditional nMOS or pMOS input stage for VLT OTA designs. The measured THD for 5-mV_{pp} input is lower than -61 dB. An integrated noise of 0.65 μV_{rms} in the frequency band of 0.3–200 Hz) for the LFP signal acquisition and 2.14 μV_{rms} in the frequency band of 0.2 k–5 kHz for the AP signal acquisition is achieved, respectively. The measured NEF of 2.37 (0.3–200 Hz) and 1.56 (0.2 k–5 kHz) are one of the lowest in the literature.

References

[1] S. J. Bensmaia and L. E. Miller, "Restoring sensorimotor function through intracortical interfaces: Progress and looming challenges," *Nature Rev. Neurosci.*, vol. 15, no. 5, pp. 313–325, Apr. 2014.

[2] M. Pais-Vieira *et al.*, "A Closed loop brain-machine interface for epilepsy control using dorsal column electrical stimulation," *Sci. Rep.*, vol. 6, Sep. 2016, Art. no. 32814.

[3] E. C. Leuthardt, G. Schalk, J. R. Wolpaw, J. G. Ojemann, and D. W. Moran, "Journal of neural engineering a brain–computer interface using electrocorticographic signals in humans," *J. Neural Eng.*, vol. 1, no. 2, pp. 63–71, Jun. 2004.

[4] M. A. Lebedev and M. A. L. Nicolelis, "Brain–machine interfaces: Past, present and future," *Trends Neurosci.*, vol. 29, no. 9, pp. 536–546, Sep. 2006.

[5] X. Liu, M. Zhang, A. G. Richardson, T. H. Lucas, and J. Van der Spiegel, "Design of a closed-loop, bidirectional brain machine interface system with energy efficient neural feature extraction and PID control," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 4, pp. 729–742, Aug. 2017.

[6] A. Bagheri, M. T. Salam, J. L. P. Velazquez, and R. Genov, "Low-frequency noise and offset rejection in DC-coupled neural amplifiers: A review and digitally-assisted design tutorial," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 1, pp. 161–176, Feb. 2017.

[7] H. Chandrakumar and D. Marković, "An 80-mV_{pp} linear-input range, 1.6-ΩG input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mV_{pp} common-mode interference," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2811–2828, Nov. 2017.

[8] T. M. Seese, H. Harasaki, G. M. Saidel, and C. R. Davies, "Characterization of tissue morphology, angiogenesis, and temperature in the adaptive response of muscle tissue to chronic heating," *Lab. Invest., J. Tech. Methods Pathol.*, vol. 78, no. 12, pp. 1553–1562, Dec. 1998.

[9] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.

[10] C. Qian, J. Parramon, and E. Sánchez-Sinencio, "A micropower low-noise neural recording front-end circuit for epileptic seizure detection," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1392–1405, Jun. 2011.

[11] F. Zhang, J. Holleman, and B. P. Otis, "Design of ultra-low power biopotential amplifiers for biosignal acquisition applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 4, pp. 344–355, Aug. 2012.

[12] L. Shen, N. Lu, and N. Sun, "A 1-V 0.25-ÂμW inverter stacking amplifier with 1.07 noise efficiency factor," *IEEE J. Solid-State Circuits*, vol. 53, no. 3, pp. 896–905, Mar. 2018.

[13] V. Majidzadeh, A. Schmid, and Y. Leblebici, "Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 3, pp. 262–271, Jun. 2011.

[14] T.-Y. Wang, M.-R. Lai, C. M. Twigg, and S.-Y. Peng, "A fully reconfigurable low-noise biopotential sensing amplifier with 1.96 noise efficiency factor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 3, pp. 411–422, Jun. 2014.

[15] T. Denison, K. Consoer, W. Santa, A. T. Avestruz, J. Cooley, and A. Kelly, "A 2 μW 100 nV/rtHz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, Dec. 2007.

[16] Q. Fan, F. Sebastiano, J. H. Huijsing, and K. A. A. Makinwa, "A 1.8μw 60 nV/$\sqrt{}$Hz capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1534–1543, Jul. 2011.

[17] U. Ha, J. Lee, M. Kim, T. Roh, S. Choi, and H.-J. Yoo, "An EEG-NIRS multimodal SoC for accurate anesthesia depth monitoring," *IEEE J. Solid-State Circuits*, vol. 53, no. 6, pp. 1830–1843, Jun. 2018.

[18] M. A. B. Altaf, C. Zhang, and J. Yoo, "A 16-channel patient-specific seizure onset and termination detection SoC with impedance-adaptive transcranial electrical stimulator," *IEEE J. Solid-State Circuits*, vol. 50, no. 11, pp. 2728–2740, Nov. 2015.

[19] C. Qian, J. Shi, J. Parramon, and E. Sánchez-Sinencio, "A low-power configurable neural recording system for epileptic seizure detection," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 4, pp. 499–512, Aug. 2013.

[20] H. Rezaee-Dehsorkh, N. Ravanshad, R. Lotfi, K. Mafinezhad, and A. M. Sodagar, "Analysis and design of tunable amplifiers for implantable neural recording applications," *IEEE Trans. Emerg. Sel. Topics Circuits Syst.*, vol. 1, no. 4, pp. 546–556, Dec. 2011.

[21] R. Muller *et al.*, "A minimally invasive 64-channel wireless μECoG implant," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 344–359, Jan. 2015.

[22] B. Linares-Barranco and T. Serrano-Gotarredona, "On the design and characterization of femtoampere current-mode circuits," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1353–1363, Aug. 2003.

[23] J. Silva-Martinez and J. Salcedo-Suñer, "IC voltage to current transducers with very small transconductance," *Analog Integr. Circuits Signal Process.*, vol. 13, no. 3, pp. 285–293, Jul. 1997.

[24] M. Steyaert, P. Kinget, and W. Sansen, "Full integration of extremely large time constants in CMOS," *Electron. Lett.*, vol. 27, no. 10, pp. 790–791, May 1991.

[25] A. Arnaud, R. Fiorelli, and C. Galup-Montoro, "Nanowatt, sub-nS OTAs, with sub-10-mV input offset, using series-parallel current mirrors," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2009–2018, Sep. 2006.

[26] H. Chandrakumar and D. Marković, "A simple area-efficient ripple-rejection technique for chopped biosignal amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 2, pp. 189–193, Feb. 2015.

[27] H. Kassiri *et al.*, "Rail-to-rail-input dual-radio 64-channel closed-loop neurostimulator," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 2793–2810, Nov. 2017.

[28] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "Sub-μV_{rms}-noise sub-μW/channel ADC-direct neural recording with 200-mV/ms transient recovery through predictive digital autoranging," *IEEE J. Solid-State Circuits*, vol. 53, no. 11, pp. 3101–3110, Nov. 2018.

[29] J. Lee, H. Kim, and S. Cho, "A 255 nW ultra-high input impedance analog front-end for non-contact ECG monitoring," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr./May 2017, pp. 1–4.

[30] S. Lee *et al.*, "A 110dB-CMRR 100dB-PSRR multi-channel neural-recording amplifier system using differentially regulated rejection ratio enhancement in 0.18 μm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 472–474.

[31] C. M. Lopez *et al.*, "An implantable 455-active-electrode 52-channel CMOS neural probe," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 248–261, Jan. 2014.

[32] F. M. Yaul and A. P. Chandrakasan, "A sub-μw 36nv/$\sqrt{}$Hz chopper amplifier for sensors using a noise-efficient inverter-based 0.2V-supply input stage," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb. 2016, pp. 94–95.

[33] C. Kim, S. Joshi, H. S. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "A 92 dB dynamic range sub-μV_{rms}-noise 0.8 μW/ch neural-recording ADC array with predictive digital autoranging," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 470–472.

[34] S.-Y. Park, J. Cho, K. Na, and E. Yoon, "Modular 128-channel Δ-$\Delta\Sigma$ analog front-end architecture using spectrum equalization scheme for 1024-channel 3-D neural recording microsystems," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 501–514, Feb. 2018.

[35] S.-Y. Park, J. Cho, and E. Yoon, "3.37 μW/Ch modular scalable neural recording system with embedded lossless compression for dynamic power reduction," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C168–C169.

[36] U. Ha *et al.*, "A 25.2 mW EEG-NIRS multimodal SoC for accurate anesthesia depth monitoring," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 450–451.

[37] K. A. Ng and Y. P. Xu, "A multi-channel neural-recording amplifier system with 90 dB CMRR employing CMOS-inverter-based OTAS with CMFB through supply rails in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[38] H. Chandrakumar and D. Markovic, "A 2.8 μW 80 mV_{pp}-linear-input-range 1.6Gω-input impedance bio-signal chopper amplifier tolerant to common-mode interference up to 650 mV_{pp}," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 448–449.

[39] H. Chandrakumar and D. Marković, "A 2μW 40 mV_{pp} linear-input-range chopper-stabilized bio-signal amplifier with boosted input impedance of 300 Mω and electrode-offset filtering," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan./Feb. 2016, pp. 96–97.

[40] S. Mondal, C.-L. Hsu, R. Jafari, and D. Hall, "A dynamically reconfigurable ecg analog front-end with a 2.5$\times$ data-dependent power reduction," in *Proc. IEEE Custom Integr. Circuits Conf.*, Apr./May 2017, pp. 1–4.

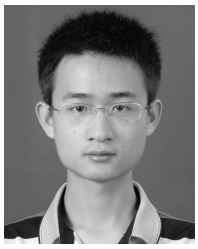
[41] U. Ha and H.-J. Yoo, "An EEG-NIRS ear-module SoC for wearable drowsiness monitoring system," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2016, pp. 193–196.

[42] W. A. Smith, J. P. Uehlin, S. I. Perlmutter, J. C. Rudell, and V. S. Sathe, "A scalable, highly-multiplexed delta-encoded digital feedback ECoG recording amplifier with common and differential-mode artifact suppression," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. C172–C173.

[43] S.-J. Kim, L. Liu, L. Yao, W. L. Goh, Y. Goh, and M. Je, "A 0.5-V sub-μW/channel neural recording IC with delta-modulation-based spike detection," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Nov. 2014, pp. 189–192.

[44] U. Ha *et al.*, "A wearable EEG-HEG-HRV multimodal system with real-time tES monitoring for mental health management," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[45] J. Xu *et al.*, "A 0.6 V 3.8 μW ECG/bio-impedance monitoring IC for disposable health patch in 40 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Apr. 2018, pp. 1–4.



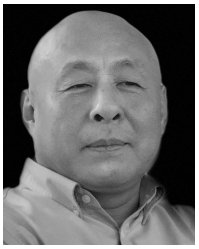
Deng Luo (S'16) received the B.S. degree in electronic engineering from the Huazhong University of Science and Technology, Wuhan, China, in 2014. He is currently pursuing the Ph.D. degree with Tsinghua University, Beijing, China, focusing on low-noise, low-power, and low-voltage analog circuit design.

His research interests include analog and mixed-signal circuit designs, especially for biomedical applications.

Milin Zhang (S'06–M'11–SM'17) received the B.S. and M.S. degrees in electronic engineering from Tsinghua University, Beijing, China, in 2004 and 2006, respectively, and the Ph.D. degree from the Electronic and Computer Engineering Department, The Hong Kong University of Science and Technology (HKUST), Hong Kong.

She was a Post-Doctoral Researcher with the University of Pennsylvania, Philadelphia, PA, USA. In 2016, she joined the Department of Electronic Engineering, Tsinghua University, as an Assistant Professor. Her research interests include designing traditional and various nontraditional imaging sensors, such as polarization imaging sensors and focal-plane compressive acquisition image sensors. She is also interested in analog and mixed-signal circuit designs oriented for various applications.

Dr. Zhang has been serving as a Technology Program Committee Member of the IEEE Asian Solid-State Circuits Conference (A-SSCC) since 2019, the IEEE Custom Integrated Circuits Conference (CICC) since 2018, and the IEEE International Solid-State Circuits Conference Student Research Preview (ISSCC SRP) Committee. She received the Best Paper Award of the BioCAS Track of the 2014 International Symposium on Circuits and Systems (ISCAS) and the Best Paper Award (first place) of the 2015 Biomedical Circuits and Systems Conference (BioCAS).



Zhihua Wang (M'99–SM'04–F'17) received the B.S., M.S., and Ph.D. degrees in electronic engineering from Tsinghua University, Beijing, China, in 1983, 1985, and 1990, respectively.

He was a Visiting Scholar with Carnegie Mellon University, Pittsburgh, PA, USA, from 1992 to 1993 and Katholieke Universiteit Leuven, Leuven, Belgium, from 1993 to 1994. He has been serving as a Full Professor and the Deputy Director of the Institute of Microelectronics, Tsinghua University, since 1997 and 2000, respectively. He was a Visiting Professor with The Hong Kong University of Science and Technology, Hong Kong, from 2014 to 2015. He has coauthored 12 books/chapters, over 197 (514) papers in international journals (conferences), and over 246 (29) papers in Chinese journals (conferences). He holds 118 Chinese and 9 U.S. patents. His current research mainly focuses on CMOS radio frequency integrated circuit (RFIC) and biomedical applications, involving radio frequency identification (RFID), phase-locked loop, low-power wireless transceivers, and smart clinic equipment combined with leading-edge RFIC and digital image processing techniques.

Dr. Wang has been a Steering Committee Member of the IEEE Asian Solid-State Circuits Conference (A-SSCC) since 2005. He served as the Chairman for the IEEE SSCS Beijing Chapter from 1999 to 2009, an AdCom Member of the IEEE Solid-State Circuits Society (SSCS) from 2016 to 2019, a Technology Program Committee Member of the IEEE International Solid-State Circuits Conference from 2005 to 2011, the Technical Program Chair for A-SSCC 2013, a Guest Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS special issues in 2006, 2009, and 2014, an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I AND II and the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and other administrative/expert committee positions in China's national science and technology projects.